A 10 Gb/s Clock and Data Recovery System in 90nm CMOS

Final Project Report

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ECEN 620: Broadband Circuit Design

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1. Motivation and Overview

The demand for high-speed intersystem communications in settings like data centers is growing rapidly. Further, the need for power and cost-efficient circuits is high, motivating the development of high-speed link circuits that can transmit, receive, and decode data being transmitted in a way that is resistant to external factors such as noise, temperature, and supply voltage variations.

On the receive side specifically, clock and data recovery systems (CDRs) are often leveraged to recover a clock signal from incoming data and synchronize it to the data transitions, to ensure proper sampling margin when the data is decoded and provide a jitter-free clock signal for subsequent circuits. In addition to clock recovery, the system outputs a retimed data stream which is synchronous with the generated clock signal.

CDR systems must be able to track a certain amount of input data jitter while outputting error free, correctly retimed data. In communications standards, this is governed by a jitter tolerance (JTOL) mask, which describes how much periodic jitter the CDR should be able to track at varying frequencies of jitter. Particularly for 10Gb/s optical communications, the OC-192 (or STM-64) standard governs this requirement [1]. Other key quantities of interest in a CDR system include power consumption, nominal output clock jitter and periodicity, and bit error rate (BER) achieved.

In this project, a 10Gb/s CDR circuit is implemented in a 90nm CMOS process. Due to the relatively low f_t of this process (around 130GHz), a half-rate architecture is adopted in order to leverage the low-power operation of digital elements in the phase detector, while still generating the sufficiently fast output pulses required.

2. Literature Survey

There are numerous examples of CDR systems in literature. Many examples at data rates of 10Gb/s and beyond utilize half-rate architectures [2] [3], with a variety of phase detector architectures including binary, such as the Alexander PD, and linear, such as the Hogge PD. Some more complex examples, at 40Gb/s, include additional techniques such as decision feedback equalization (DFE), or opt to use a quarter-rate architecture for phase detection [4] [5].

Many topologies exist for phase detection of random data in CDR architectures [6]. In this project, a half-rate Alexander PD will be utilized. Thus, it is important to understand the characteristics and behavior of these topologies. The binary PD is studied in detail in literature, with analysis on its effect on loop dynamics, jitter tolerance, jitter transfer, and its linearized behavior and methods for approximating it [7] [8] [9].

3. Architecture

3.1 Overview

A block diagram of the system architecture is shown below in *Figure 1*. The system is based on an analog PLL architecture, and is half rate, that is, the data is retimed on both the rising and falling edges of the clock. This enables both the VCO and clocking in the PD to operate at half the full-rate speed. Particularly in the PD, the speed requirements of the logic gates driving the charge pump are significantly reduced. A binary Alexander PD is utilized for its higher potential speed of operation compared to a linear phase detector. A standard charge pump is driven by the PD, with a second-order loop filter to generate the control voltage for the quadrature VCO (QVCO). In the QVCO, quadrature clock phases are generated, buffered, and converted to a CMOS-type square wave to drive the PD clocking. Since the Alexander PD automatically retimes the input data, a simple mux is used to recover the retimed, full-rate data.

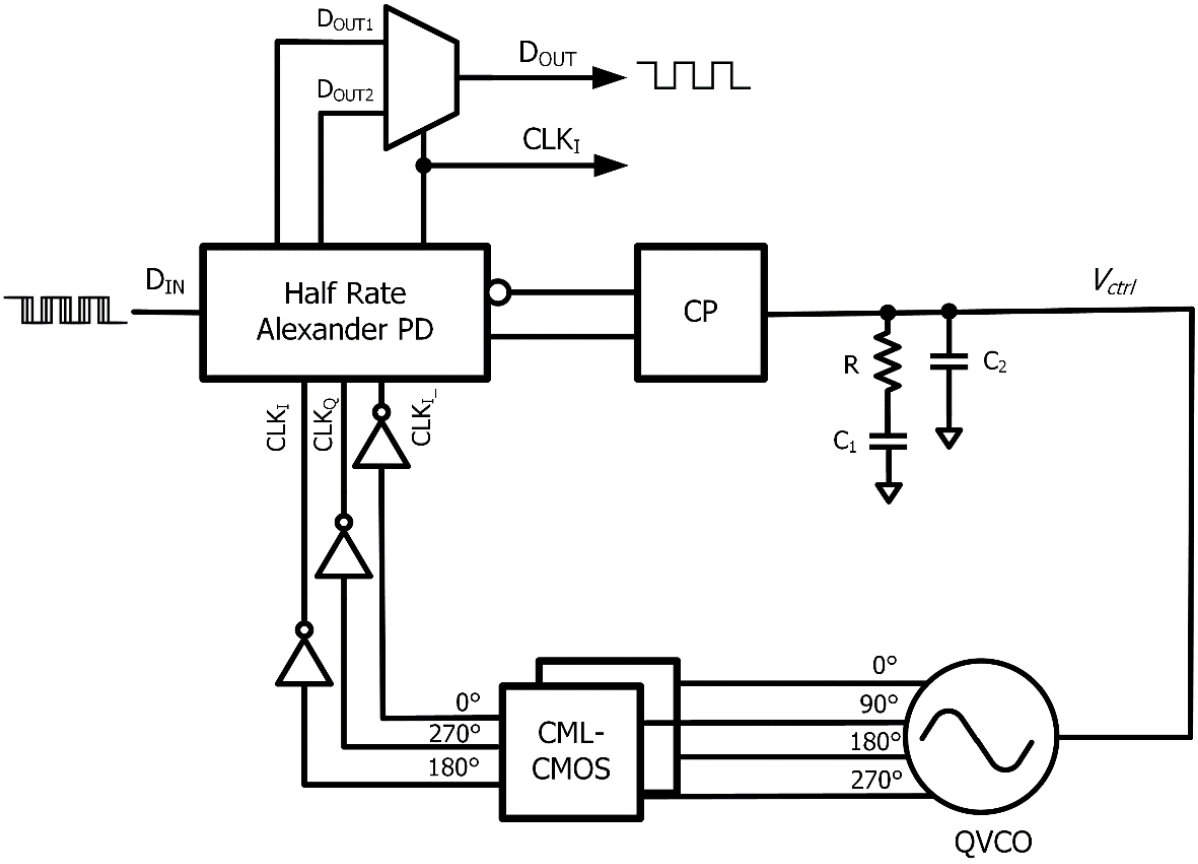

Figure 1: CDR System Block Diagram

3.2 Half-rate Alexander PD

The schematic and timing diagram of the half-rate Alexander PD is shown below in *Figure 2*. The topology consists of three flip-flops which sample the data at three of the quadrature clocks' rising edges, generating control signals A1, A2, A3, which are then compared to generate the early or late signal to drive the charge pump. The locked state is when the rising edge of CK_Q is in the vicinity of the data transitions. In reality, the PD will lock with a small static phase offset due to the clock-to-Q delay through the flip-flops. In this architecture, since the VCO gain is effectively negative with respect to the control voltage, the early and late signals are flipped to correctly drive the charge pump. In addition, the early signal is inverted since it is driving a PMOS transistor in the charge pump.

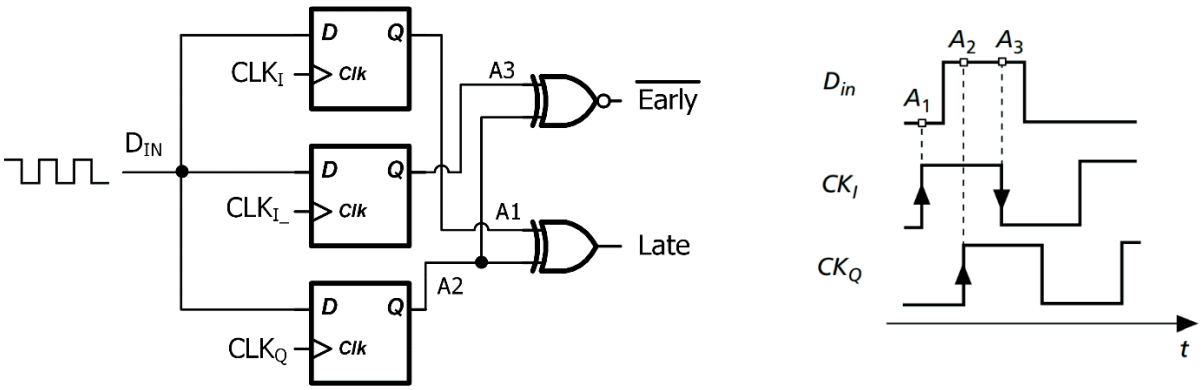

Figure 2: Half-rate Alexander PD

The D flip-flop topology is shown below in *Figure 3*. A true single-phase clock (TSPC) architecture is used for its higher speed operation and lower clock loading than a traditional latch-based flip-flop. The addition of an inversion is included to buffer the output and ensure the correct polarity of Q.

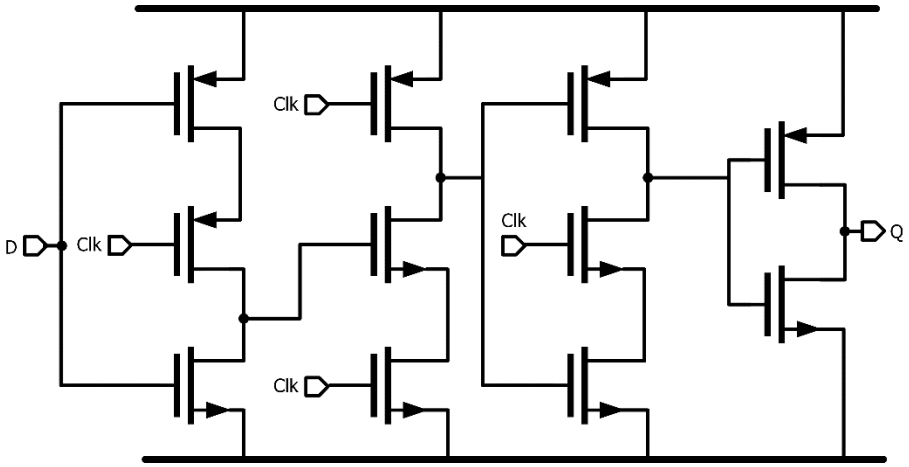

Figure 3: True Single-Phase Clock (TSPC) D Flip-Flop

To drive the charge pump, custom complementary XOR/XNOR gates are used (*Figure 4)*, due to Naseri and Timarchi [10]. The gates are higher speed than traditional XOR/XNOR gates, and most importantly, are complementary, ensuring that the delay through each gate is identical, reducing the mismatch error in the charge pump.

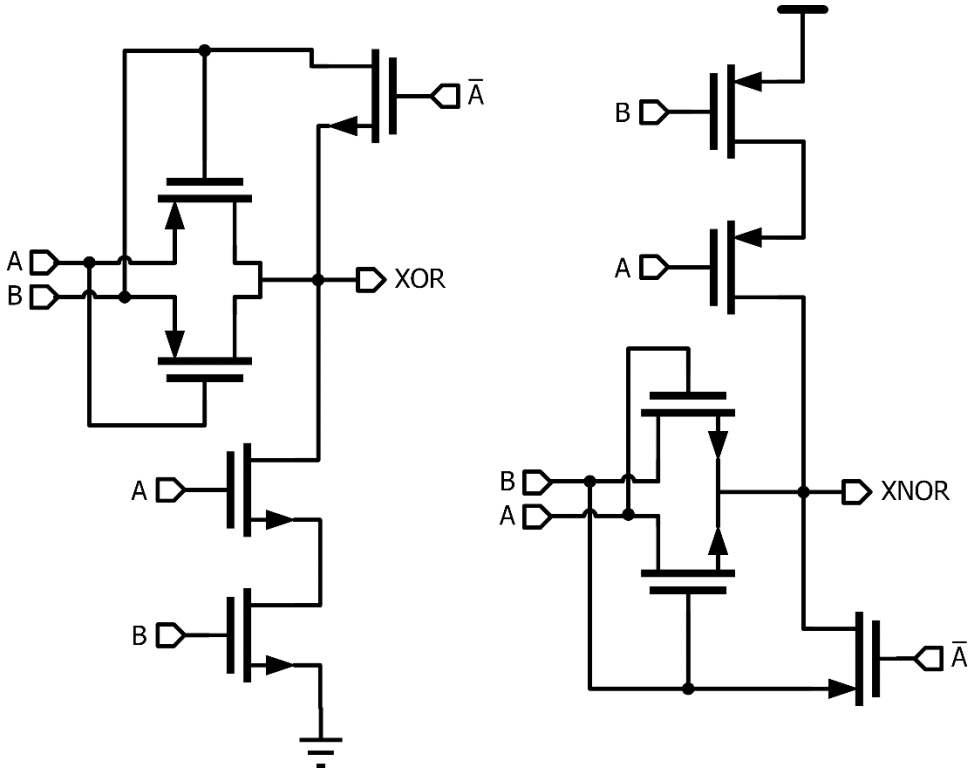

Figure 4: Complementary XOR/XNOR

3.3 Charge Pump

A relatively standard charge pump was implemented for this architecture. Since the nominal VCO frequency is around 5GHz, the charge pump was optimized for this particular control voltage. Since the clock rate should always be around 5GHz for 10Gb/s half-rate data, the control voltage should stay within a hundred millivolts of this value.

3.4 Loop Filter

A second-order loop filter was used to properly integrate the charge pump current, filter high-frequency perturbations, and ensure stable loop dynamics.

3.5 Quadrature Voltage Controlled Oscillator (QVCO)

Since the system uses a half-rate binary PD, the generation of quadrature clock outputs is necessary. To accomplish this, the use of a quadrature VCO (QVCO) based on a pair of LC-VCOs is leveraged to generate quadrature outputs at a relatively low phase noise (*Figure 5*). Traditionally, the QVCO control devices M_{cpl} are implemented as parallel devices, but literature has shown better phase noise results with the use of cascode-type devices [11], thus that topology is implemented in this project.

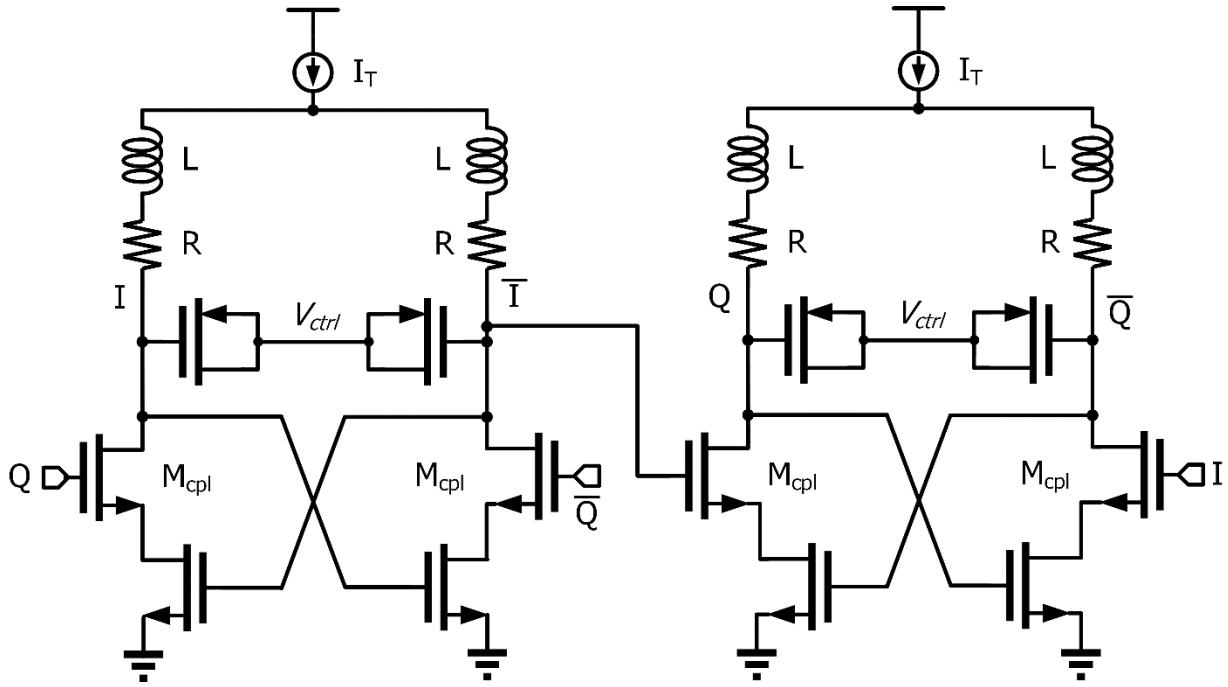

Figure 5: LC-QVCO Topology

The QVCO can be designed using two identical 5GHz VCOs with additional control devices. A typical LC-VCO can be designed using the following equations.

First, the quality factor in an inductor is equal to

$$Q = \frac{2\pi L}{R}$$

where R is the series resistance. For analysis, the series resistance and inductance can be transformed to their parallel equivalents as

$$R_P = Q^2$$

$$L_p = L\left(1 + \frac{1}{Q^2}\right)$$

In this topology, parallel PMOS varactors are used to control the VCO output frequency, along with a coarse set fixed capacitance. The capacitance in a varactor can be expressed as

$$C_P = WLC_{ox}$$

with C_{ox} being a process parameter, approximately 0.123 fF/μm^2 in this process.

In an LC tank, the frequency of oscillation can be expressed as

$$2\pi f_{osc} = \frac{1}{\sqrt{L_P C_p}}$$

where oscillation is satisfied when

$$\frac{1}{g_m} = \frac{1}{\sqrt{2k_n'\left(\frac{W}{L}\right)I_D}} \leq R_p$$

3.6 CML to CMOS Conversion

Because the QVCO outputs a CML-type sinusoidal signal, some buffering is necessary to convert the clock signals to a rail-to-rail CMOS swing with ideally fast rise times and a 50% duty cycle. Outputting a clean buffered clock is extremely important for accurate and correct phase detection and data retiming.

The topology shown in *Figure 6* is used to achieve these goals. The first CML stage amplifies the signal, allowing it to clip from a large-signal perspective, and the subsequent stage performs differential to single-ended conversion. Special care was taken in sizing this stage to ensure a close to 50% duty cycle with symmetric rise and fall times. The output is then buffered with an inverter to drive the appropriate capacitance required by the flip-flop sizing. A tail current of 1mA was used to ensure high speed operation while minimizing power consumption as much as possible.

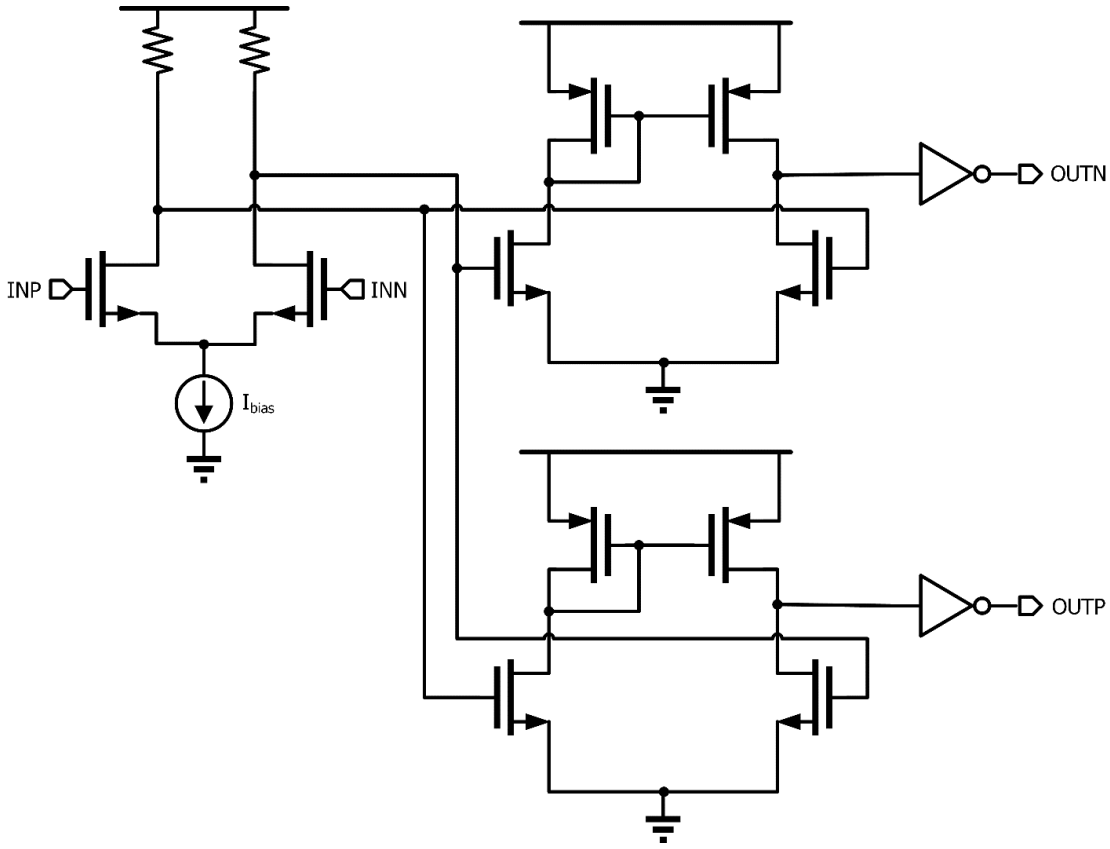

Figure 6: CML-CMOS Topology

4. Simulation Results

4.1 Linearized System Behavior

To determine the loop dynamics in the CDR, a linearized system model was first developed and tested. Notably, the Alexander PD, a non-linear element, was linearized to approximate its behavior. The linearized s-domain model of the CDR is shown below in *Figure 7*.

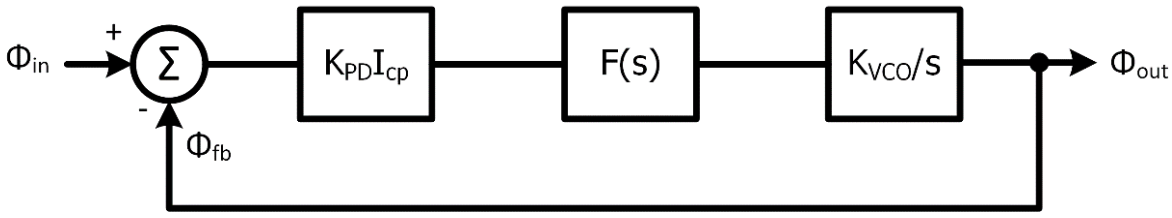

Figure 7: Linearized CDR Model

For this system, using a second-order loop filter, the function F(s) can be expressed as

$$F(s) = \frac{\left(\frac{1}{C_2}\right)\left(s + \frac{1}{RC_1}\right)}{s\left(s + \frac{C_1 + C_2}{RC_1C_2}\right)}$$

The closed loop transfer function H(s) and loop gain LG(s) can be derived as

$$H(s) = \frac{\phi_{out}}{\phi_{in}}(s) = \frac{\frac{K_{PD}I_{cp}K_{VCO}}{C_2}\left(s + \frac{1}{RC_1}\right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2}\right)s^2 + \left(\frac{K_{PD}I_{cp}K_{VCO}}{C_2}\right)s + \frac{K_{PD}I_{cp}K_{VCO}}{RC_1C_2}}$$

$$LG(s) = \frac{K_{PD}I_{cp}F(s)K_{VCO}}{s} = \frac{K_{PD}I_{cp}K_{VCO}\left(s + \frac{1}{RC_1}\right)}{C_2s^2\left(s + \frac{C_1 + C_2}{RC_1C_2}\right)}$$

In general, when input jitter is present, the gain in an Alexander PD can be approximated as

$$K_{PD} = \frac{2}{J_{pp}}(TD)$$

where J_{pp} is the input peak-to-peak jitter in radians, and TD is the transition density. To obtain a more accurate value, including effects from non-idealities such as clock rise/fall times and flip-flop metastability, the PD gain was obtained in simulation. The PD gain plot of average integrated output voltage over delay is shown in *Figure 8*. The approximate gain at lock, during the rising edge of the pulse shown, was found to be 2.09.

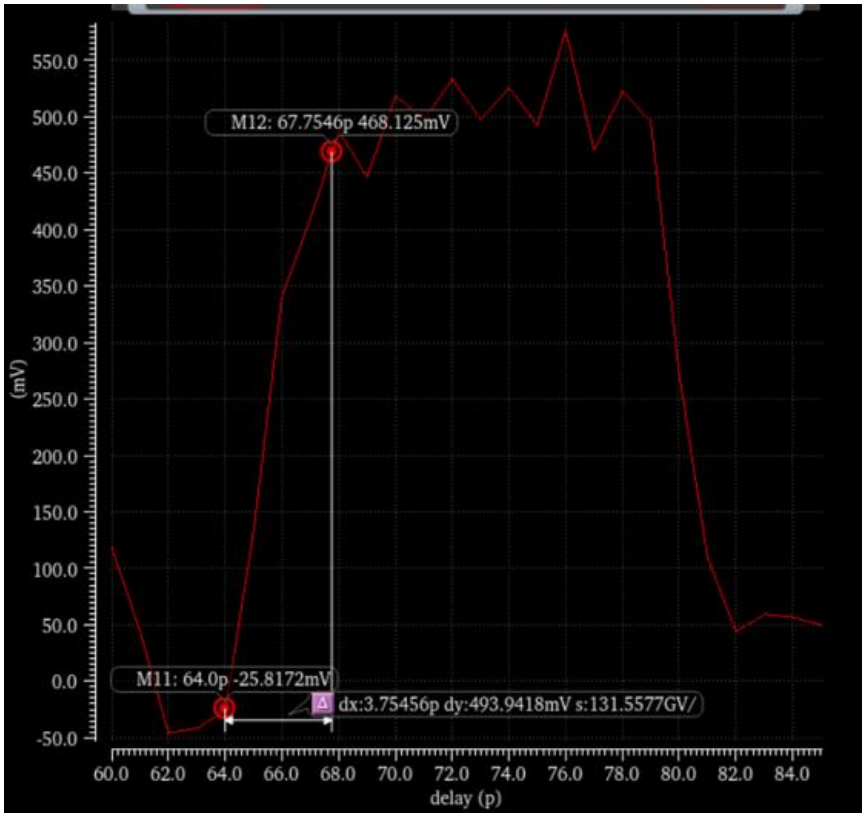

Figure 8: Alexander PD Simulated Linearized Gain

Now with an approximation for the PD gain, the loop dynamics can be studied and optimized using linearized analysis. The desired loop specifications are shown in *Table 1*, and the design procedure is described below. A large phase margin of 80° is chosen to reduce peaking in the closed loop response, and compensate for the reduction in PD gain when input jitter is present. A 3-dB frequency of 6MHz is chosen to ensure the system can track jitter at sufficiently high frequencies, up to around 4MHz.

Table 1: Loop Behavior Specifications

Specification	**Target Value**
Phase Margin	80°
f_u	5 MHz
K_{pd}	2.09/rad
f_{3dB}	6 MHz

The following analog PLL design procedure can be used to optimize the phase margin for this third-order system [12].

First, using the desired phase margin, the ratio between loop capacitors is found as

$$K_C = \frac{C_1}{C_2} = 2\left(\tan^2\phi_m + tan\phi_m\sqrt{\tan^2\phi_m + 1}\right) = 129.65$$

Next, letting R=4kΩ, the remaining capacitor values are set based on K_c and ω_u

$$\omega_z = \frac{\omega_u}{\sqrt{1 + K_C}}$$

$$C_1 = \frac{1}{\omega_z R} = 82.7pF$$

$$C_2 = \frac{C_1}{K_C} = 637.8fF$$

Lastly, the charge pump current is set to achieve the desired loop gain.

$$I_{cp} = \frac{C_2 \omega_u^2}{K_{VCO}} \sqrt{\frac{\omega_{p3}^2 + \omega_u^2}{\omega_z^2 + \omega_u^2}} = 2.9\mu A$$

The open loop response is shown below in *Figure 9*. The design achieves an 80° phase margin as desired.

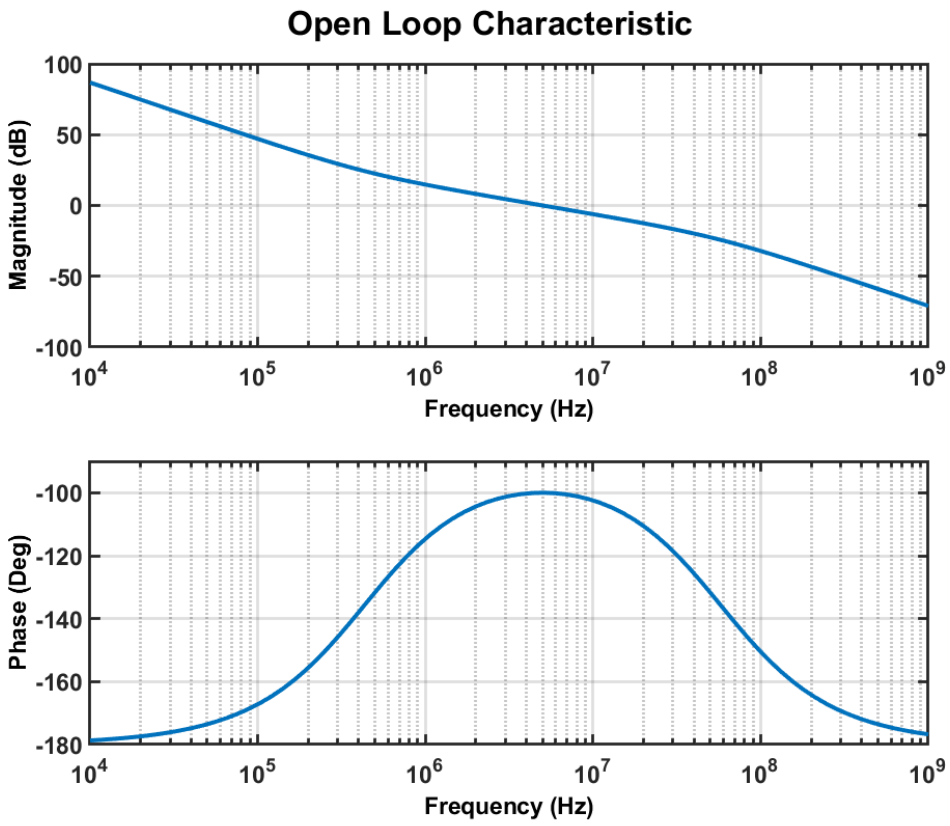

Figure 9: Open Loop Response

The closed loop response is shown below in *Figure 10*. The design achieved the desired 3-dB bandwidth of approximately 6MHz, with minimized peaking to reduce jitter transfer.

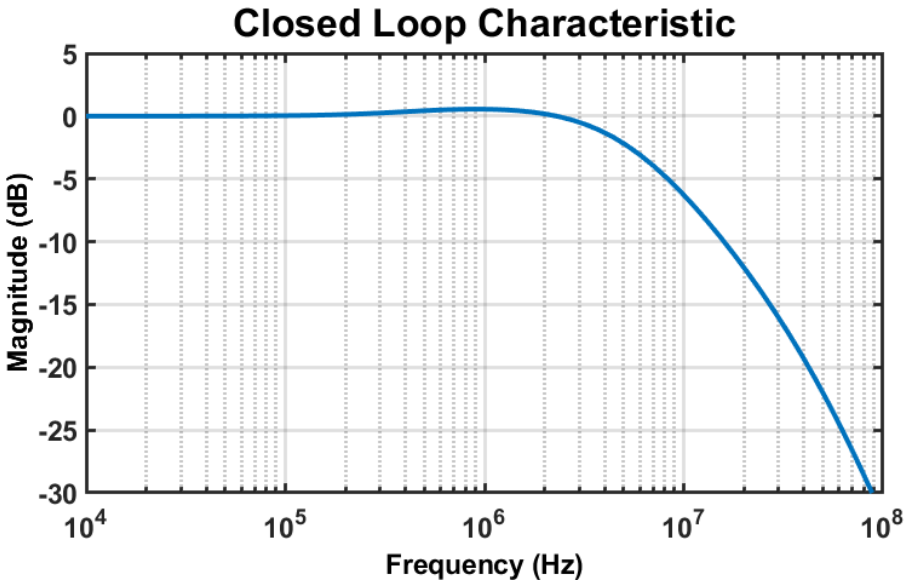

Figure 10: Closed Loop Magnitude Response

The ideal jitter tolerance curve is shown in *Figure 11*, with the OC-192 mask outlined in black. In reality, this behavior is deteriorated at high jitter frequencies due to reduction in the overall loop gain, but was found to be relatively accurate at lower jitter frequencies.

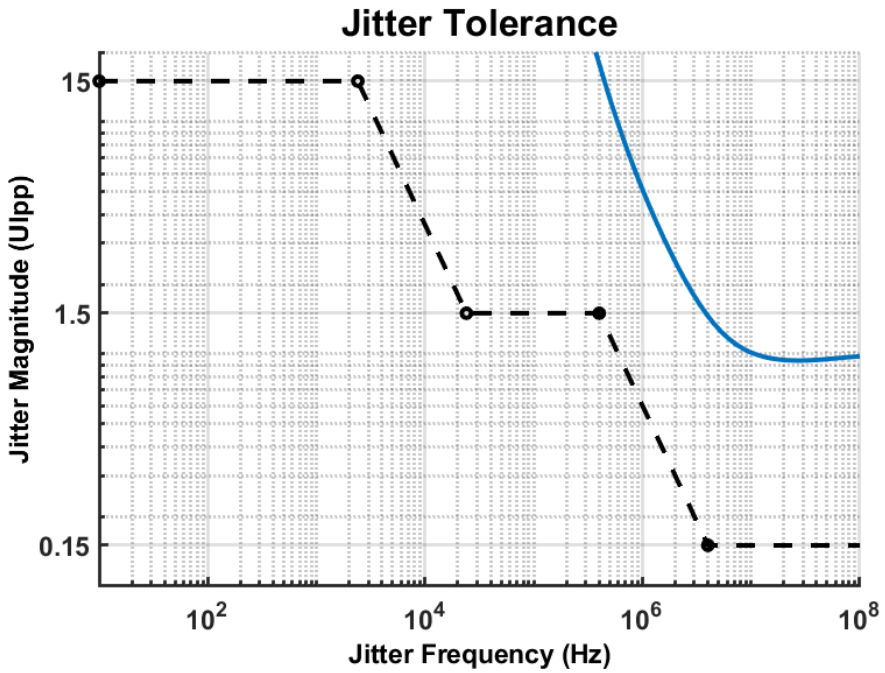

Figure 11: Ideal Jitter Tolerance (blue) with OC-192 Mask (black)

4.2 Half-rate Alexander PD

Next, the phase detector was verified for ideal clock inputs. The sample waveforms are shown in *Figure 12*. The output XOR and XNOR gates must sustain pulse widths of about 50ps, the spacing between the quadrature clocks. As noted previously, the PD locks to Ck_Q with a small static offset, due to delays through the flip-flops.

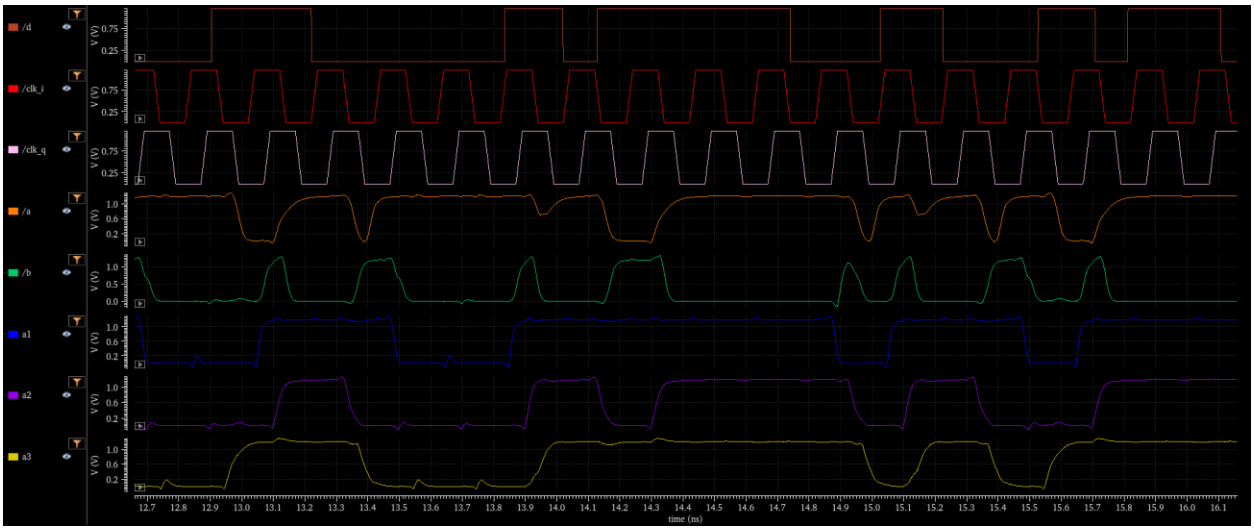

Figure 12: Sample PD Transient Behavior

4.3 Quadrature Voltage Controlled Oscillator (QVCO)

Table 2: QVCO Results

Parameter	Value
K_{VCO}	2π*1GHz/V
Phase Noise @ 1MHz Offset	-108.2 dBc
Tuning Range	4.45 – 5.65 GHz

The LC-based QVCO was designed using the procedure outlined in the previous section. The tuning range was designed for a VCO gain of roughly 1GHz/V, with nominal operation at the center control voltage of about 5GHz. A summary of the design results are included in *Table 2*. By utilizing the cascode-style quadrature control devices, slightly lower phase noise results were achieved. The VCO design offers a good tradeoff between power consumption, which will be discussed later, and phase noise performance. The use of a solid VCO is important to reduce the clock jitter and increase the jitter tolerance of the overall CDR system.

The transient response of the QVCO is shown in *Figure 13.* The phase noise measurement is shown in *Figure 14*, and the tuning range in *Figure 15.*

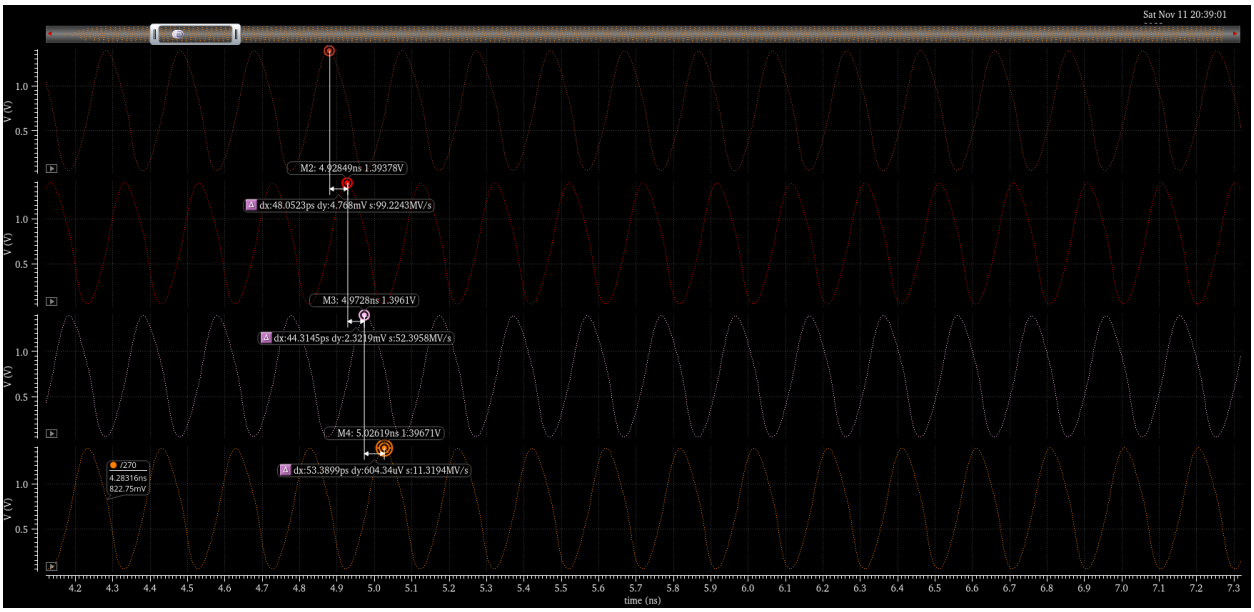

Figure 13: QVCO Transient Response

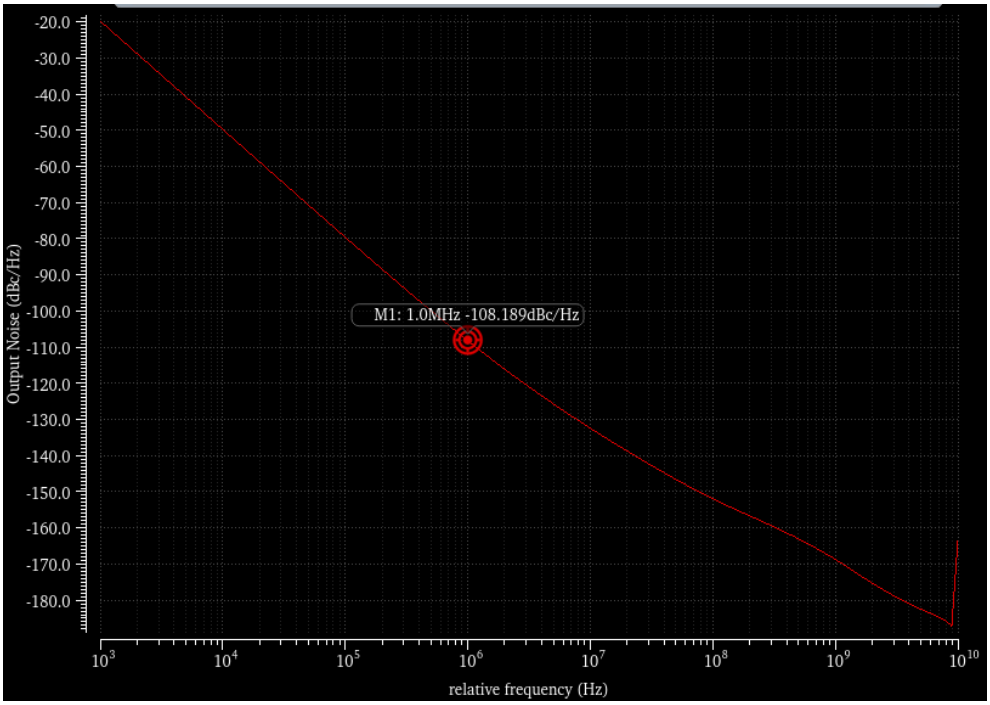

Figure 14: QVCO Phase Noise

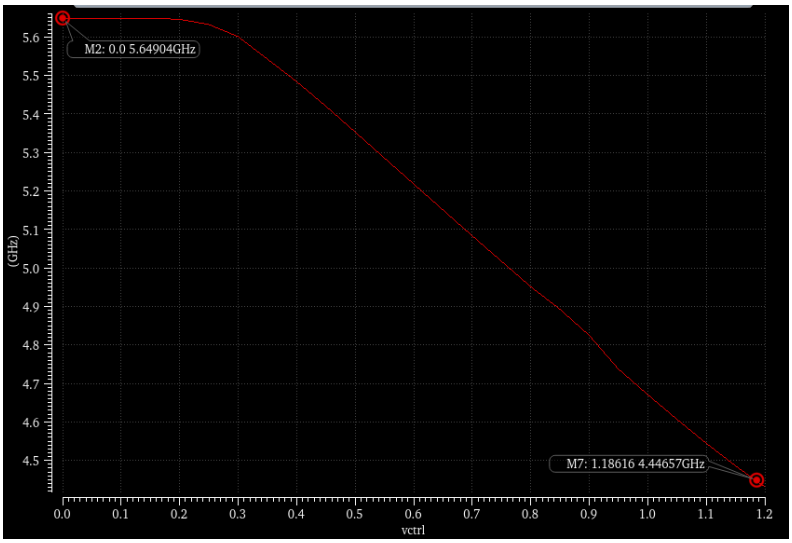

Figure 15: QVCO Tuning Range

4.4 System Performance

With all the CDR components working properly, the system was tested as a whole in feedback configuration. The test bench is shown in *Figure 16*. The CDR was simulated with an input pseudorandom bit sequence (PRBS), with a pattern length of 2^{31}-1 bits (PRBS31). In addition, 25ps of rise and fall time were added to the input data to simulate channel losses.

Table 3: CDR Performance Comparison

Work	Data Rate	Process Technology	PD Architecture	Clock Jitter (pk-pk)	JTOL	Power	BER
This work	10 Gbps	90nm CMOS	Half-rate binary	8.7ps	0.6UIpp @ 4MHz	10.7 mW	10^{-4} (error free)
[2]	10 Gbps	180nm CMOS	Half-rate binary PFD	9.9ps	N/A	91 mW	10^{-9}
[3]	10 Gbps	180nm CMOS	Half-rate linear PD	14.5ps	N/A	72 mW	$1.28*10^{-6}$
[4]	40 Gbps	180nm CMOS	Quarter-rate binary PD	9.67ps	N/A	144 mW	10^{-6}
[5]	40 Gbps	45nm CMOS	Half-rate charge steering	$0.515ps_{rms}$	0.45UIpp @ 5MHz	14 mW	10^{-12}

The CDR performance is summarized in *Table 3*. The design achieves an output clock jitter of 8.7ps peak-to-peak, a jitter tolerance of 0.6UIpp at 4MHz, and a power consumption of 10.7mW with a 1.2V supply. Comparisons to key references are also made. Due to simulation time constraints, the system was only tested to a BER of 10^{-4}, but nevertheless was completely error free.

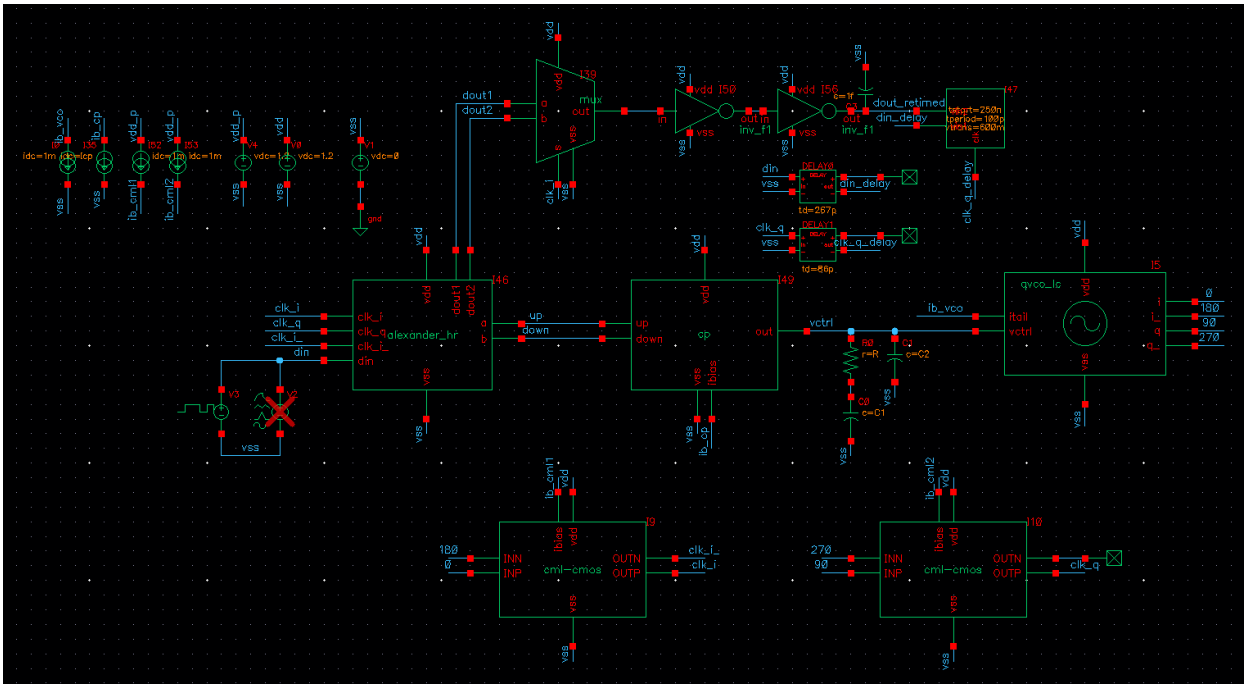

Figure 16: CDR Test Bench

The transient behavior when the CDR is locked is shown in *Figure 16.* The output data has some delay with respect to the input data due to delays through the PD, mux, and additional buffering. The lock time varied as a function of input data jitter but was generally around 200-300ns when the initial control voltage was set to about 700mV (around a 5GHz QVCO output). In a CDR system that should tolerate multiple data rates, a second loop would be added to set the coarse control voltage to around the desired frequency, then allow the phase detector to takeover and make fine adjustments as needed. In this case, since the CDR is only operating at 10 Gb/s, the control voltage can be set to the 5GHz level immediately with something like a voltage DAC.

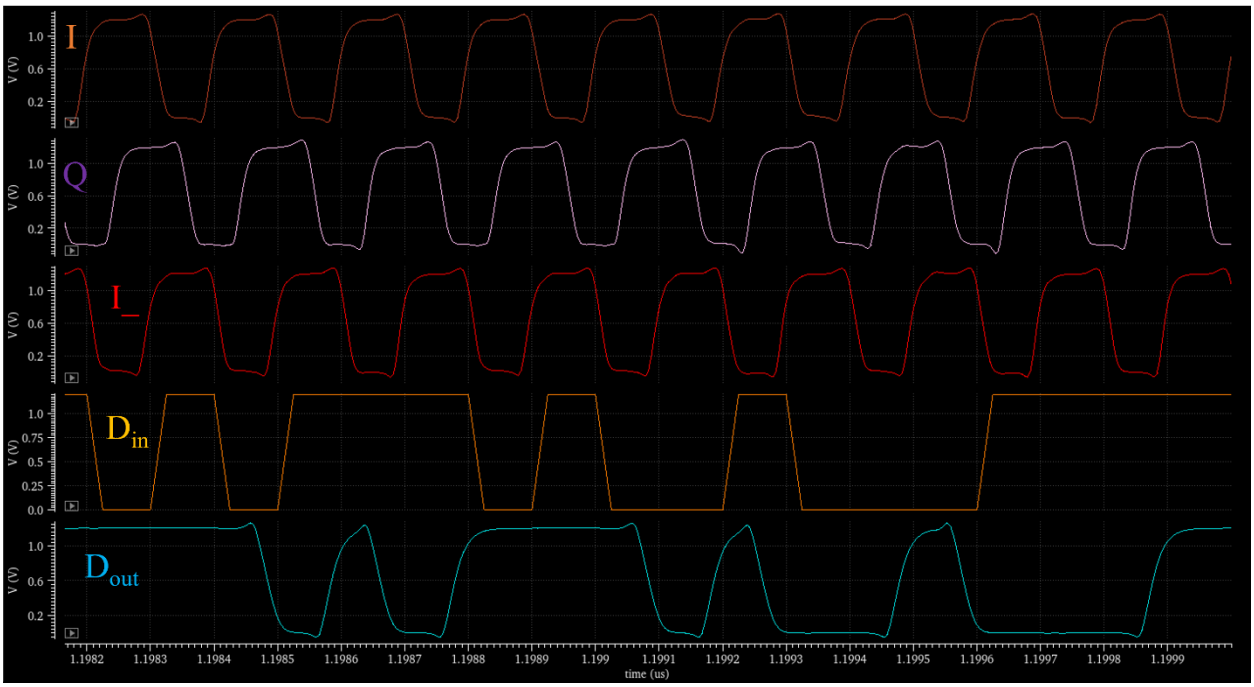

Figure 17: Sample Nominal Locked CDR Behavior

The differential, in-phase clock eye diagram and jitter are shown in *Figure 18.* This is for a simulation time of 1.2us. The clock output jitter is 8.7ps peak-to-peak, or 0.087UI. The output differential data eye diagram is included in *Figure 19.* Significant falling edge jitter was measured, perhaps due to charge-sharing on the output node of the TSPC flip-flops.

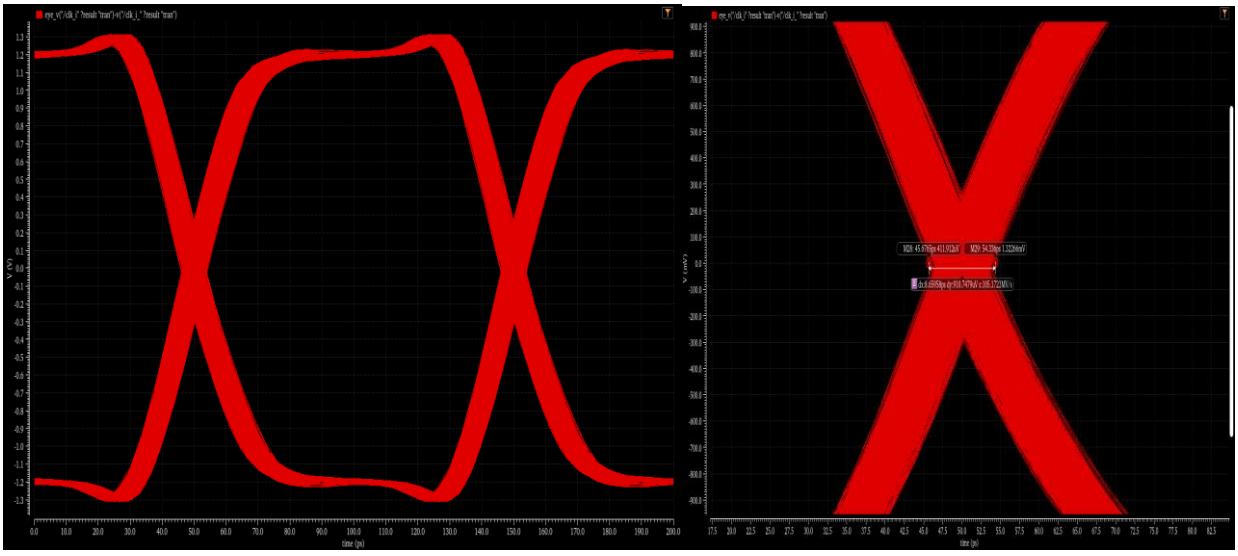

Figure 18: Differential Clock Eye Diagram and Jitter

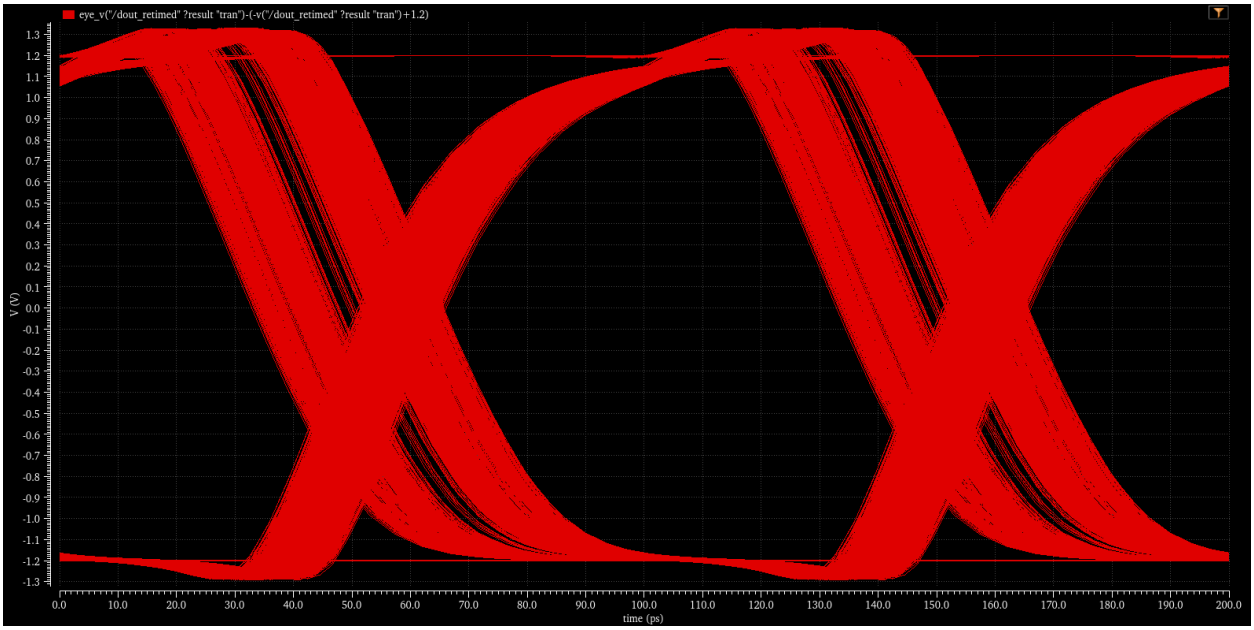

Figure 19: Differential Output Data Eye Diagram

The CDR system power consumption is summarized in *Table 4* and the pie chart below (*Figure 20).* The two dominant sources of power consumption were the QVCO and CML-CMOS buffers. The remaining digital elements were relatively low power comparatively.

Table 4: CDR Power Consumption Breakdown

Source	Power Consumption
QVCO	5.676mW
CML-CMOS Buffers	4.596mW
Alexander PD	313uW
Multiplexer	14uW
Charge Pump	8uW

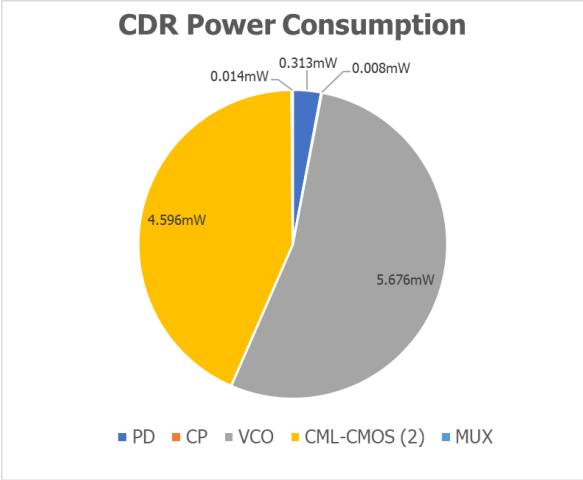

Figure 20: CDR Power Breakdown

4.5 Jitter Tolerance

Jitter tolerance is a key specification which describes how much input data jitter the CDR loop can tolerate without outputting errors. To characterize the CDR this way in simulation, a special test setup was used (*Figure 21*). The output data (from the PD) was multiplexed, buffered, and passed into a custom Verilog-A BERT cell. Once the CDR had locked, after about 200ns, the output data was compared to a delayed version of the input data (to match the delay through the PD) on the rising and falling edge of Clk_Q to ensure an ideal timing margin. The Verilog-A code for the cell is included in the appendix.

For each data point of input jitter magnitude and frequency, the circuit was simulated for a period of 1.2us, producing an error-free BER of 10^{-4}. Ideally, a BER of at least 10^{-9} is desired, but due to simulation runtime limitations this could not be reached. Nevertheless, for each data point the results were completely error free.

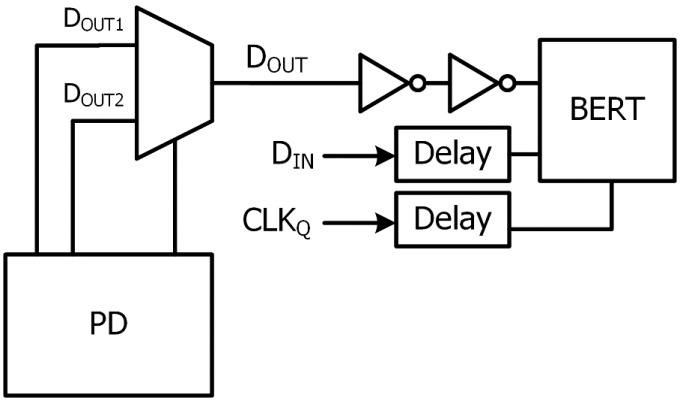

Figure 21: Jitter Tolerance Test Setup

Examples of modulating the input data jitter are shown in *Figure 22*. Sample waveforms for a case both with and without errors are shown in *Figure 23*. Note that in the error-free case there is a delay from input data to output data.

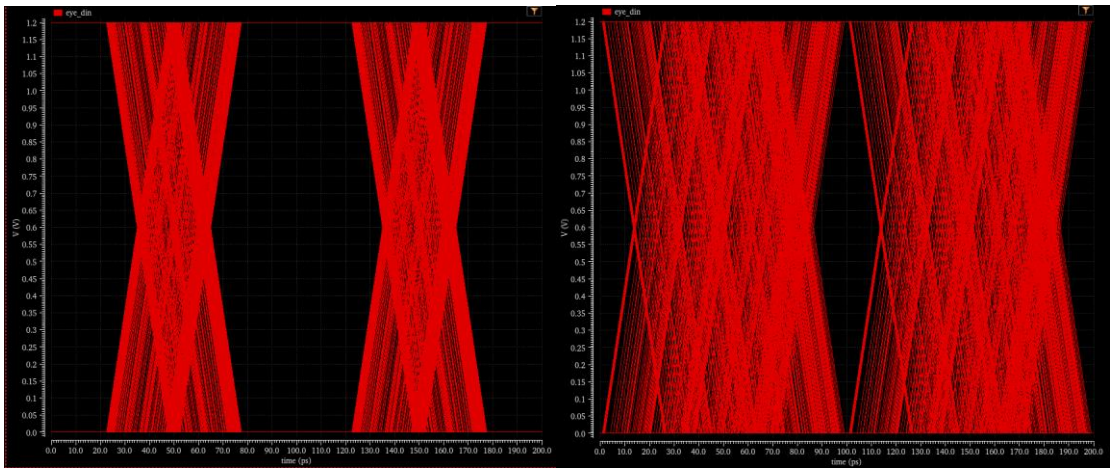

Figure 22: Sample Input Data Jitter (0.3UIpp left; 0.7UIpp right)

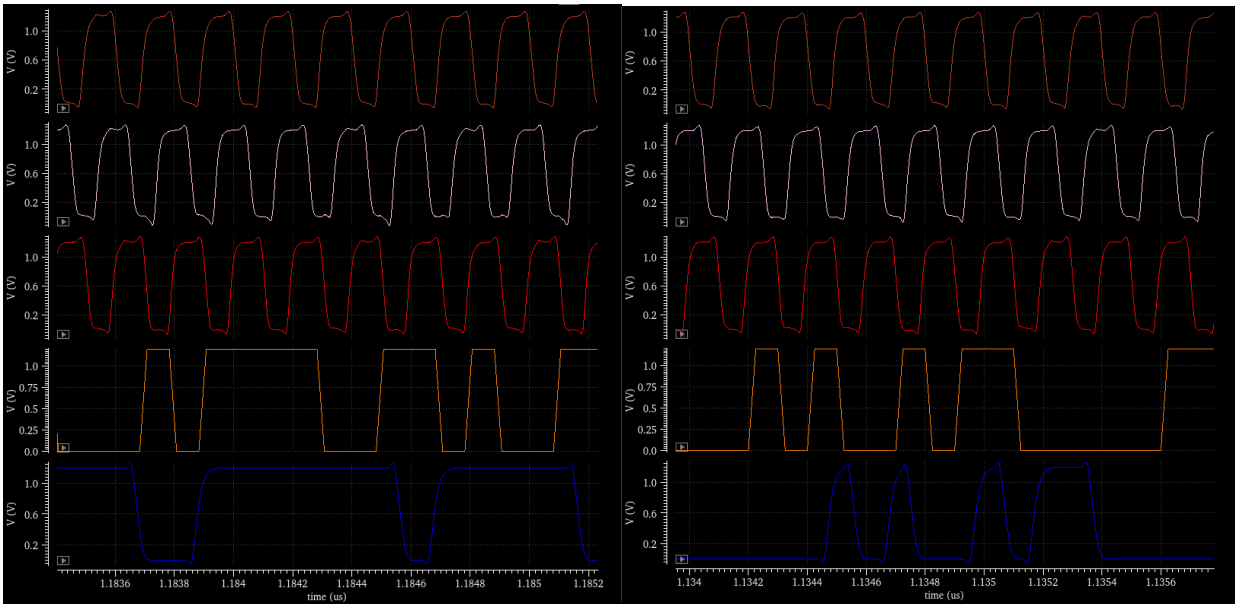

Figure 23: Sample Bit Error Comparison - Errors Present (left); Error Free (right)

The simulated jitter tolerance results are summarized in *Figure 24* and *Table 5*. Overall, the CDR was able to tolerate jitter well above the OC-192 specification. For the lower jitter frequencies, some limitation does exist due to the finite simulation time, but the behavior does line up with what was expected and measured at the higher frequencies, where many full periods of jitter can be simulated.

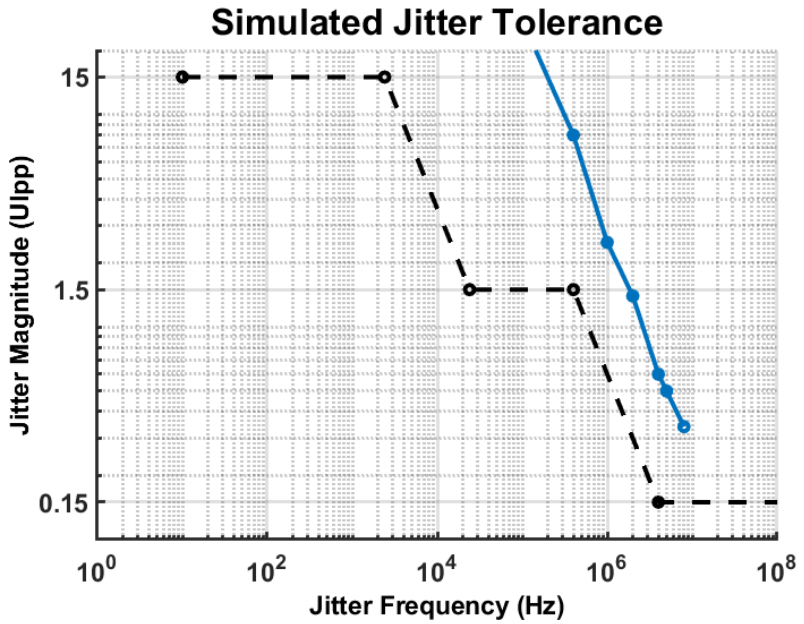

Figure 24: Simulated Jitter Tolerance (blue) and OC-192 Mask (black)

Table 5: Simulated Jitter Tolerance Points

Jitter Frequency	Jitter Tolerance (UIpp)
8 MHz	0.34
5 MHz	0.5
4 MHz	0.6
2 MHz	1.4
1 MHz	2.5
400 kHz	8
24 kHz	100

5. Conclusion

In this project, a clock and data recovery (CDR) circuit was designed in a 90nm CMOS process. The architecture includes a half-rate binary phase detector architecture, and a 5GHz quadrature VCO. The circuit successfully performs phase-locking and data regeneration at 10Gb/s, achieving an output clock peak-to-peak jitter of 8.7ps. Notably, the circuit passes the SONET OC-192 jitter tolerance specification for 10Gb/s optical systems. The power consumption is relatively low in simulation, at 10.7mW.

References

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Appendix

Design Parameters

Table 6: Schematic Fanout Values

Schematic Variable	Value
FO_A1	7.75
FO_A2	9.17
FO_A3	2.68
FO_XNOR	2.5
FO_DFF	8
FO_XOR	1

Table 7: Loop Filter Values

Parameter	Value
C1	82.7pF
C2	638fF
Icp	2.9uA
R	4kΩ

Schematic Screenshots (with sizing)

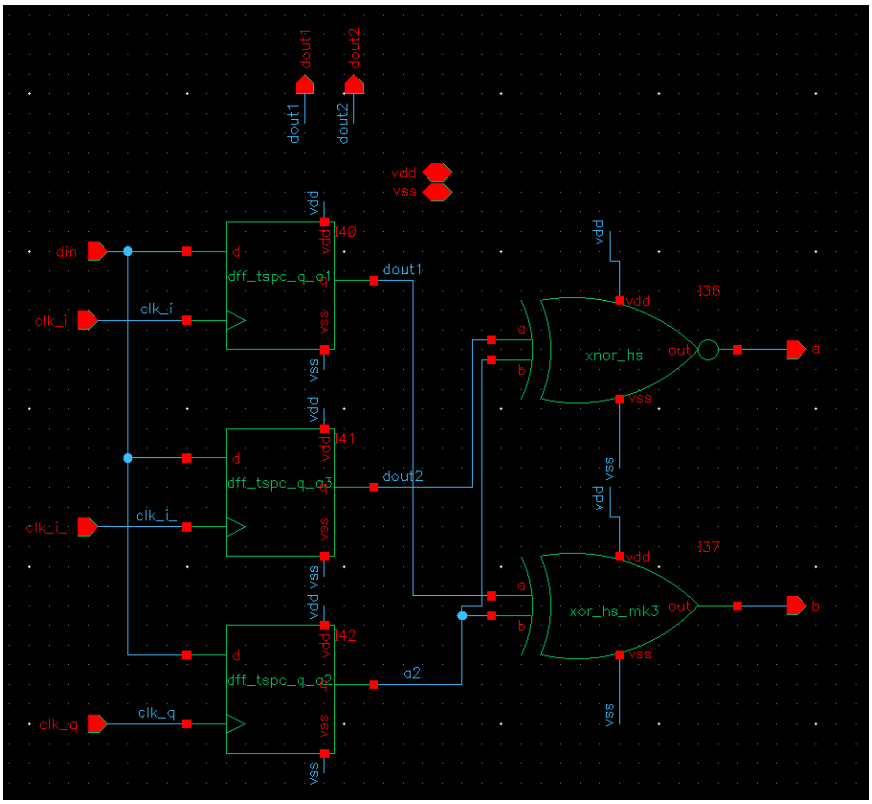

Figure 25: Alexander PD

```
module bit_error_rate (vin1, vin2, clk);
input vin1, vin2, clk;
electrical vin1, vin2, clk;
parameter real tstart  = 0 from [0:inf);
parameter real tperiod = 1 from (0:inf);
parameter real vtrans = 0.5;

   real tnext;
   integer started = 0;

   integer bits;
   integer errors;

   analog begin
     @ (timer(tstart)) started = 1;
      @ ( cross(V(clk) - vtrans,0)) begin
       if (started == 1) begin
         if ((V(vin1) > vtrans) != (V(vin2) > vtrans)) begin
            errors = errors + 1;
             $display("Bit error!",tnext);
        end
        bits = bits + 1;
      end
     end

     @ ( final_step ) begin
       if (errors == 0)
            $strobe("No errors detected :), BER=%g",1/(1.0*bits));
      else if (bits > 0 )
        $strobe( "%m: bits measured = %d, bit errs detected = %d, bit err rate = %g.\n",bits,errors,errors/(1.0*bits) );
       else
        $strobe( "No bits detected!!");
     end

   end

endmodule
```

Figure 26: BERT Verilog-A Code

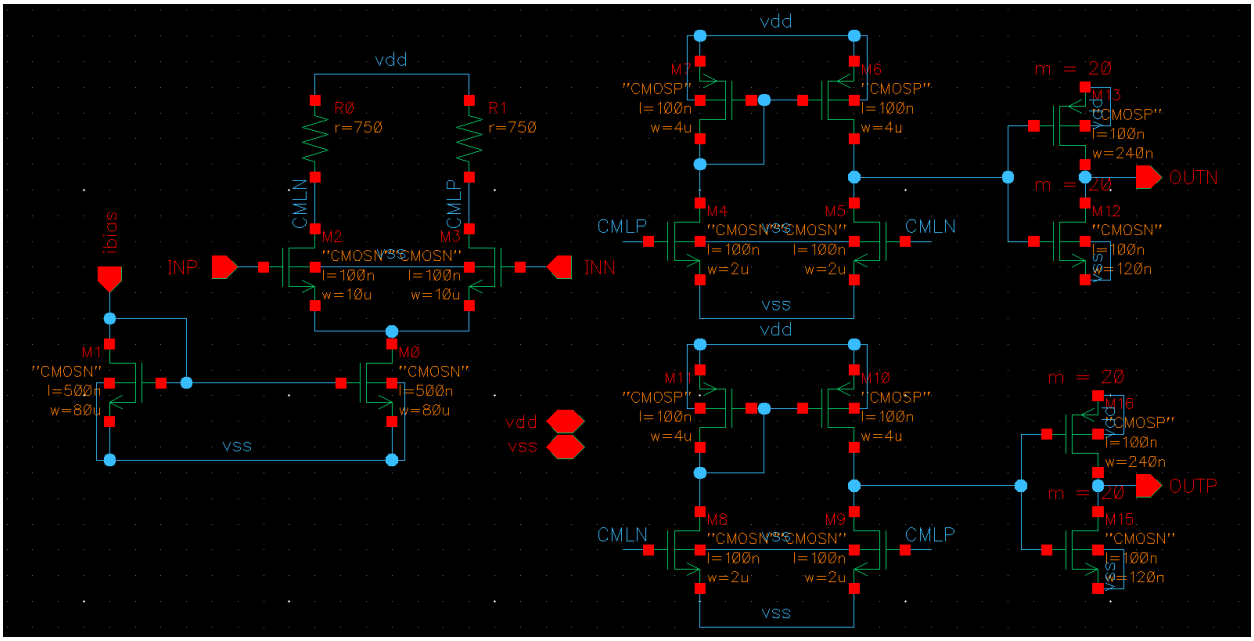

Figure 27: CML-CMOS

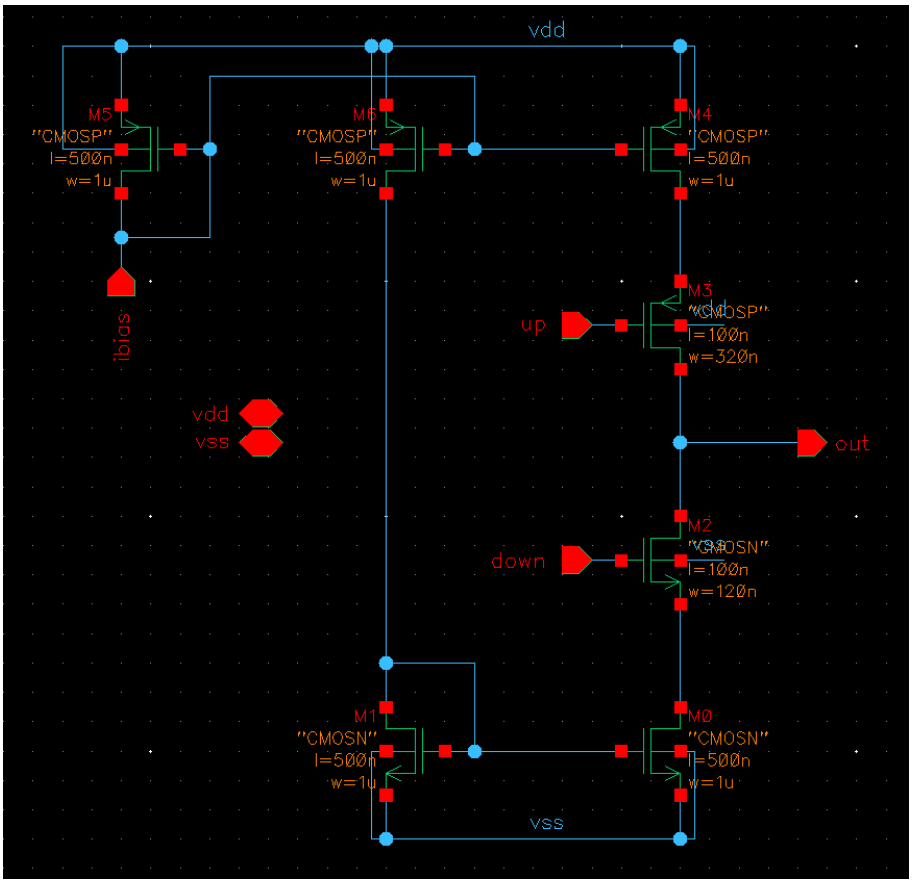

Figure 28: Charge Pump

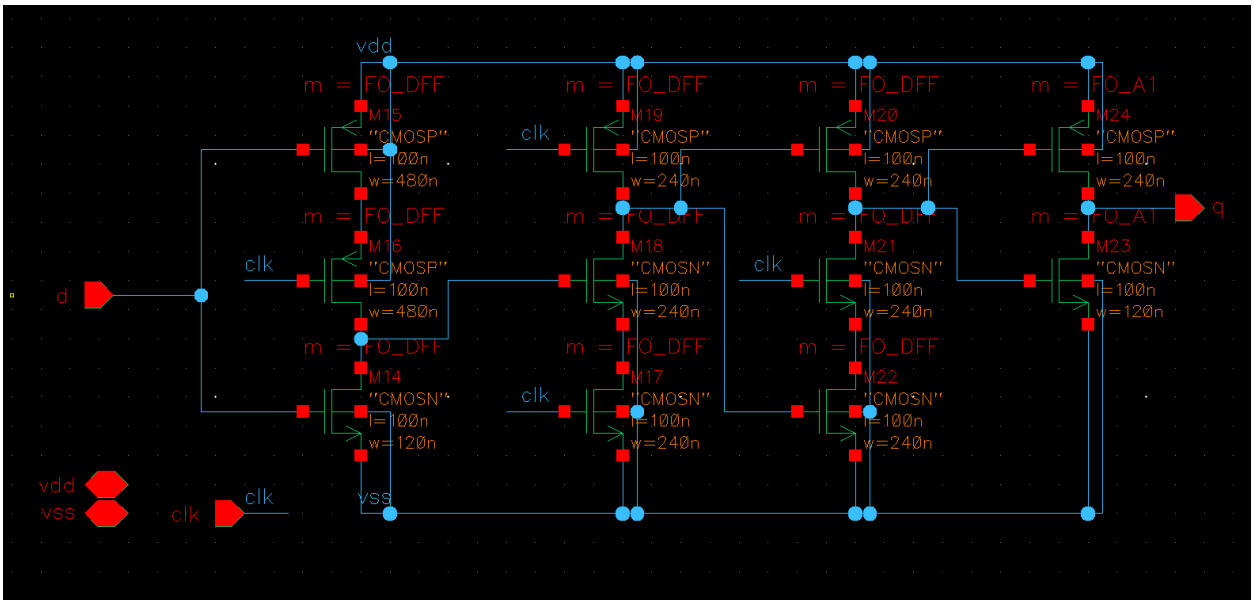

Figure 29: TSPC DFF

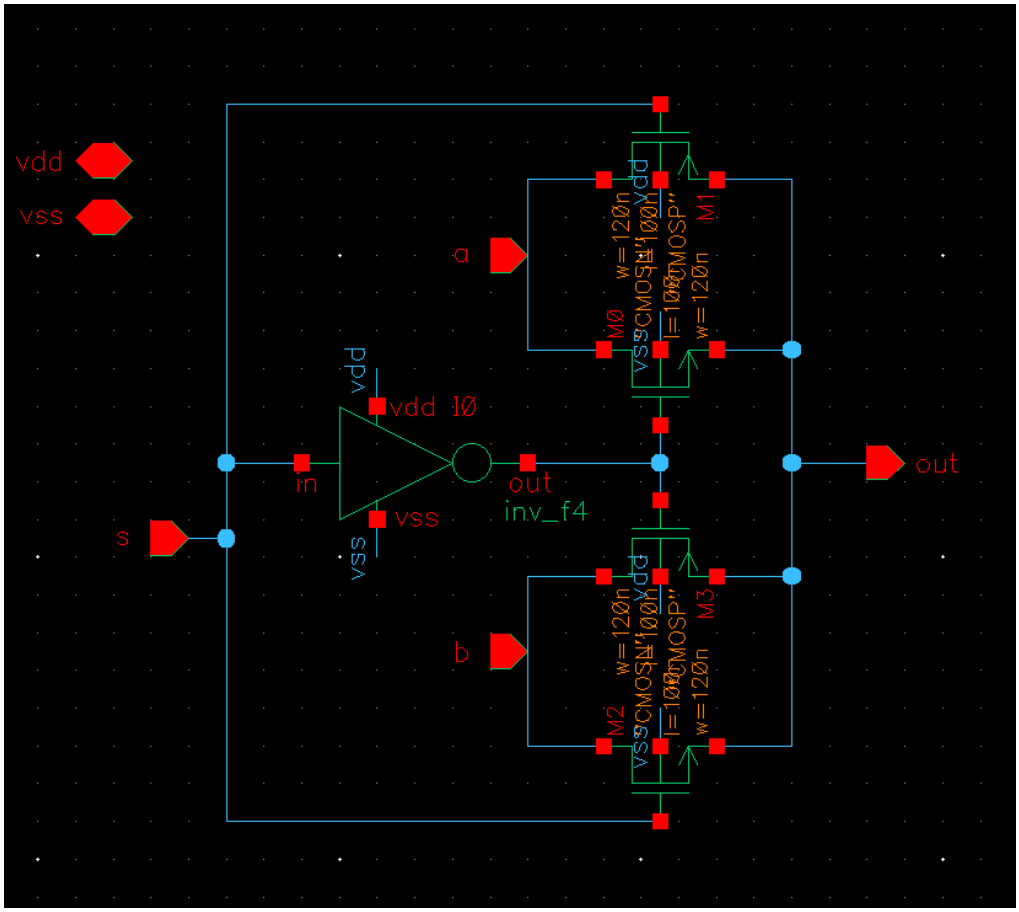

Figure 30: Multiplexer

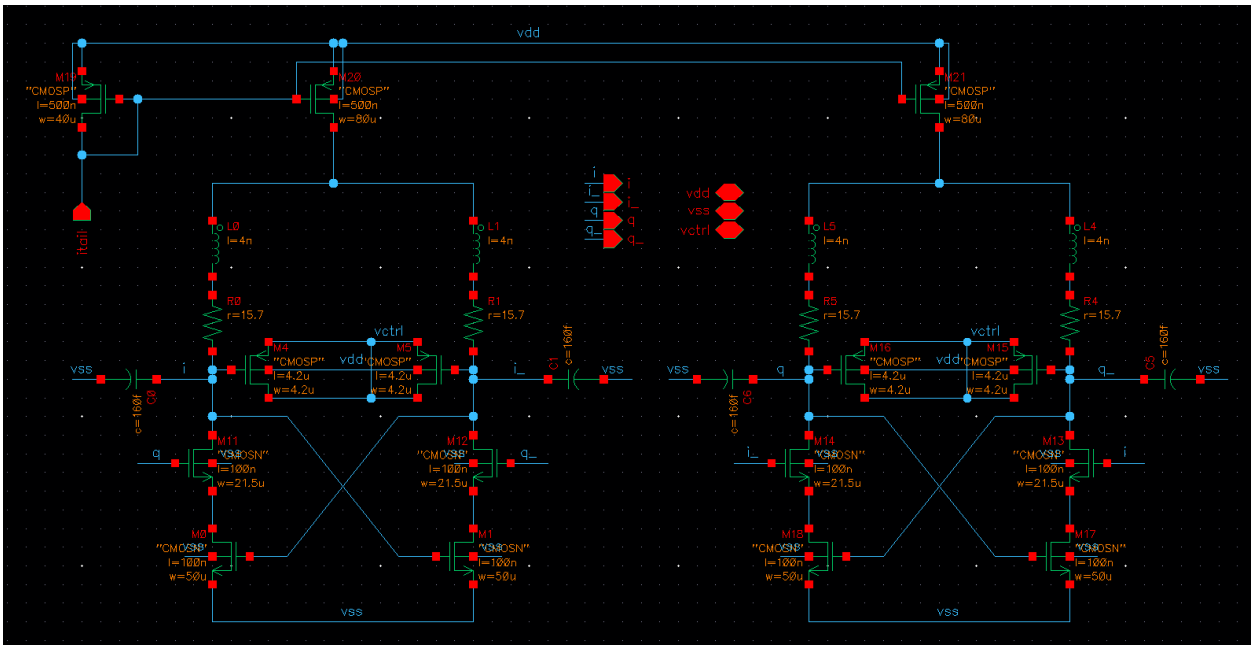

Figure 31: LC-QVCO

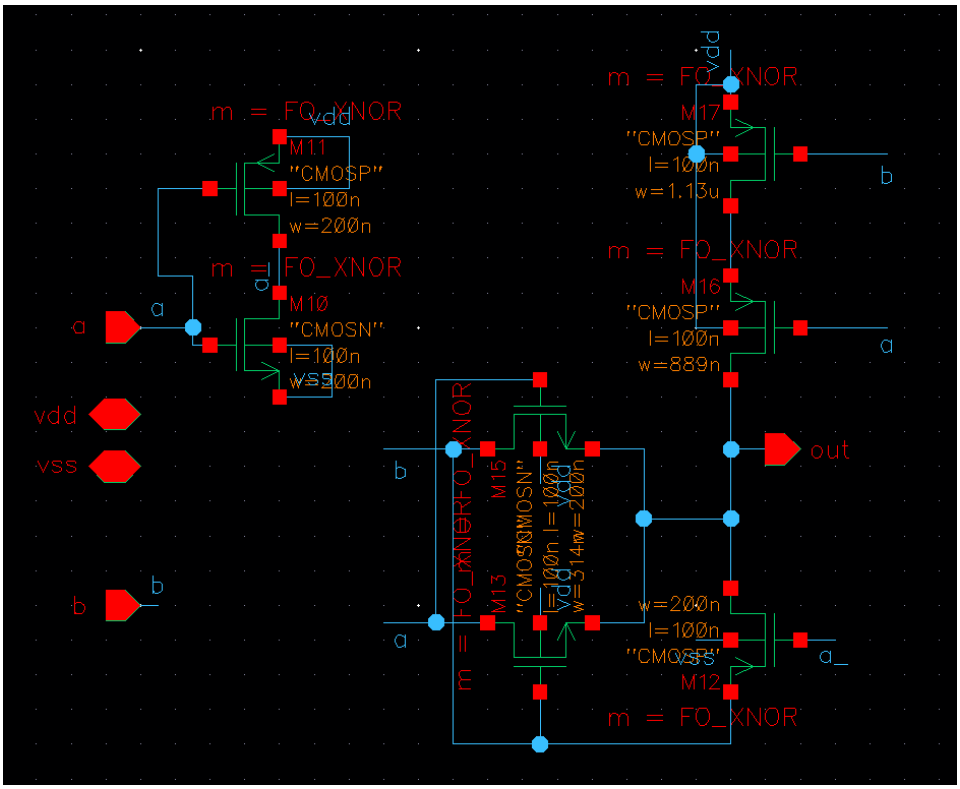

Figure 32: XNOR Gate

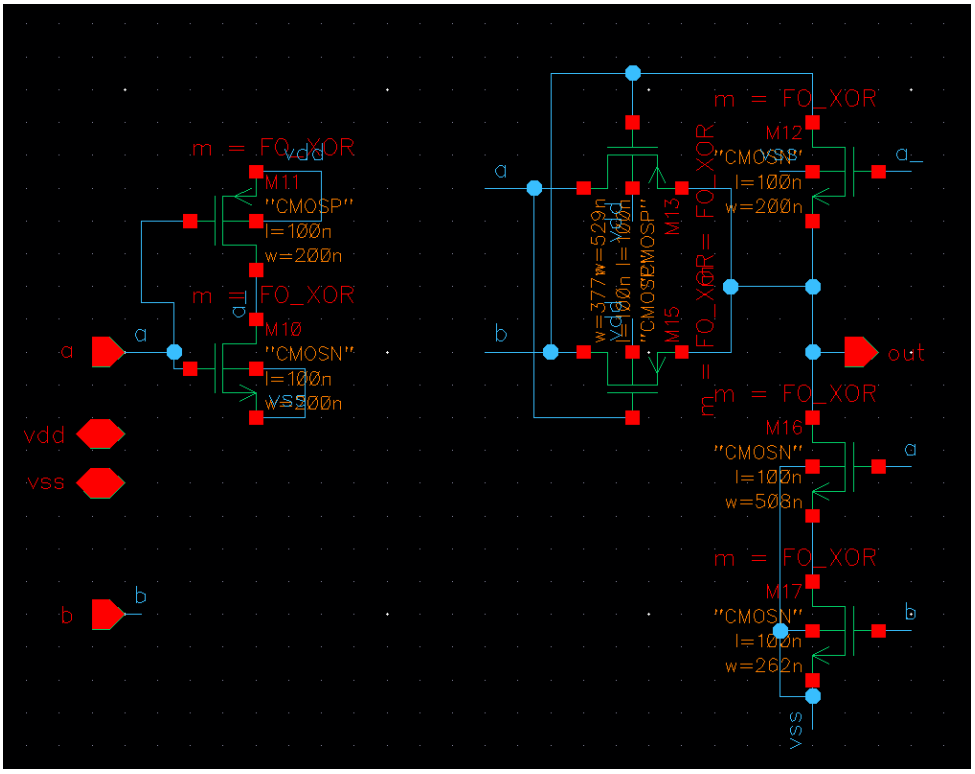

Figure 33: XOR Gate