A High-Swing, Bipolar Class-AB Amplifier for 8Ω Speaker Applications

ECEN 489 – Audio Engineering
Final Project Report

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Alex Anderson

Abstract

In this report, the design of a high-swing bipolar audio amplifier with a class-AB output stage is discussed. The amplifier drives an 8Ω load at a maximum output power of $4W_{RMS}$ (around 80% rail-to-rail). The total harmonic distortion (THD) achieved is 0.035% at a $1W_{RMS}$ output. The design was verified in simulation and measured with a physical speaker, the Dayton Audio CE81PF-8. Auditory observations are also provided.

1. Background

1.1. Output Stages

In amplifiers for audio applications, low impedance loads must be driven - around 30-50Ω for headphones and 4-8Ω for speakers. Thus, specialized output stages are needed to deliver the necessary power to the load without compromising gain and linearity of the system.

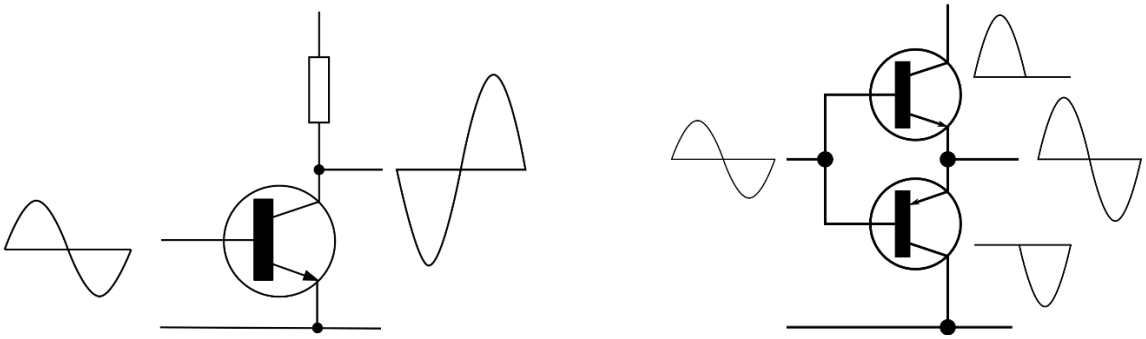

Figure 1: Class-A (left) and class-B (right) output stages

One such stage, a class-A topology (Figure 1), drives the load in a single ended fashion, with the output device conducting current for 100% of the output cycle. In the class-B topology, the load is driven in a differential fashion, with each device conducting current for exactly 50% of the output cycle. In this topology, while efficiency is increased greatly, the linearity is compromised due to the crossover distortion when both of the driving devices are briefly off. For this reason, a compromise between efficiency and linearity must be leveraged, the class-AB amplifier.

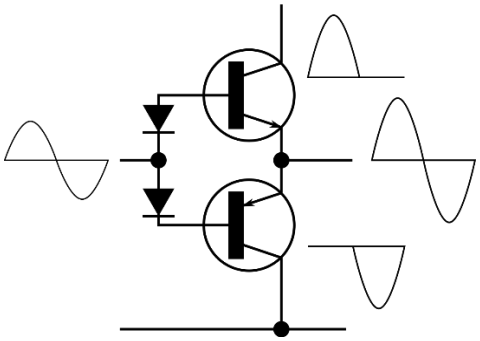

Figure 2: Class-AB output stage

In the class-AB output stage (Figure 2), a voltage bias is given to each of the output devices, causing them to conduct a small amount of DC current at all times. With this, the efficiency is

slightly reduced, but the crossover distortion is eliminated as each device now conducts current for slightly more than 50% of the output cycle. Crossover distortion can be further reduced with other techniques such as negative feedback in the system.

In a class-AB output stage, the most typical device configuration is emitter-follower, in which the NPN device is on the top side and the PNP device is on the bottom side. In this configuration, the gain of the stage is approximately unity, however the maximum voltage swing is limited by the $V_{CE,sat}$ of the two devices.

1.2. Darlington Pair

A general enhancement to BJT devices is the Darlington pair configuration [1] (Figure 3), in which the emitter of one transistor is connected to the base of another, creating a cascaded device.

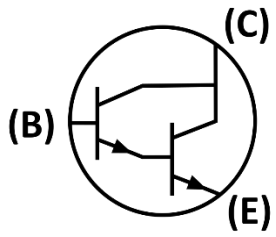

Figure 3: Darlington pair (NPN)

In this configuration, the current gain, β, of the device is boosted as

$$\beta_{tot} = \beta_1 * \beta_2 + \beta_1 + \beta_2 \cong \beta_1 * \beta_2$$

However, the effective base-emitter voltage and collector-emitter saturation voltage are shifted as

$$V_{BE,tot} = V_{BE1} + V_{BE2}$$

$$V_{CE,tot} = V_{CE1} + V_{BE2}$$

Thus, the Darlington pair offers a much higher current gain at the cost of DC headroom and a higher biasing point. Because the current gain is much higher than a single transistor, the input impedance of the device is very high, allowing for overall higher system gain. Particularly, in a cascaded application, the open loop gain of the previous amplifier will be significantly higher.

1.3. Reference Designs

One key reference design is the amplifier presented in [2]. This design uses a common-source output stage for rail-to-rail operation, with biasing circuitry to mirror the signal on the output node. While this is a monolithic CMOS implementation, the concepts are still useful for this design.

Another approach utilizes the current-mirror OTA [3]. This design includes the addition of non-linear control devices, which is not necessary for this application. The underlying topology is still useful for this design; however, an additional output stage is needed to drive the necessary output current.

2. Proposed Solution

In this section, the design considerations for the audio amplifier are discussed in detail both on the system and transistor level.

2.1. System Design

The desired system specifications are summarized in Table 1. A peak output power of at least $1W_{RMS}$ is desired, so a supply voltage of +/-10V is selected to allow for the necessary swing. A large open loop gain of at least 60dB is desired in order to have low closed loop error and thus lower distortion.

Table 1: Desired System Specifications

Specification	Value
Output Power (max)	$> 1W_{rms}$
Speaker Resistance	8Ω
Open Loop Gain	> 60dB
Phase Margin	> 45°
CL Bandwidth	> 50 kHz
THD @ $1W_{RMS}$	< 1%
V_{DD}, V_{SS}	10V, -10V

First, the required output swing can be calculated from the desired output power and load as

$$P_{out,RMS} = \frac{\left(\frac{V_{pk}}{\sqrt{2}}\right)^2}{8\Omega}$$

with an 8Ω load at $1W_{RMS}$ as desired, an output swing of +/-4V is necessary. The peak current delivered to the load can be found trivially as

$$I_{out,pk} = \frac{V_{pk}/2}{R_L} = \frac{4V}{8\Omega} = 0.5A$$

and the peak power dissipated by the output transistors is equal to

$$P_{diss} = I_{C,max}V_{CE} = (0.5A)(10V - 4V) = 3W$$

With this level of dissipation, low thermal resistance output transistors are needed with heatsinking in order to ensure overheating does not occur.

The system-level block diagram is shown below in Figure 4. It is divided into two stages: a preamplification stage for gain control and a fixed-gain stage to drive the speaker. Both stages are set up in non-inverting configuration in order to set the input and output common-mode levels symmetrically between the supply rails. The system was designed to amplify the typical line level input (around $1.4V_{pk}$) to a $1W_{RMS}$ output when the preamp stage is configured to unity gain.

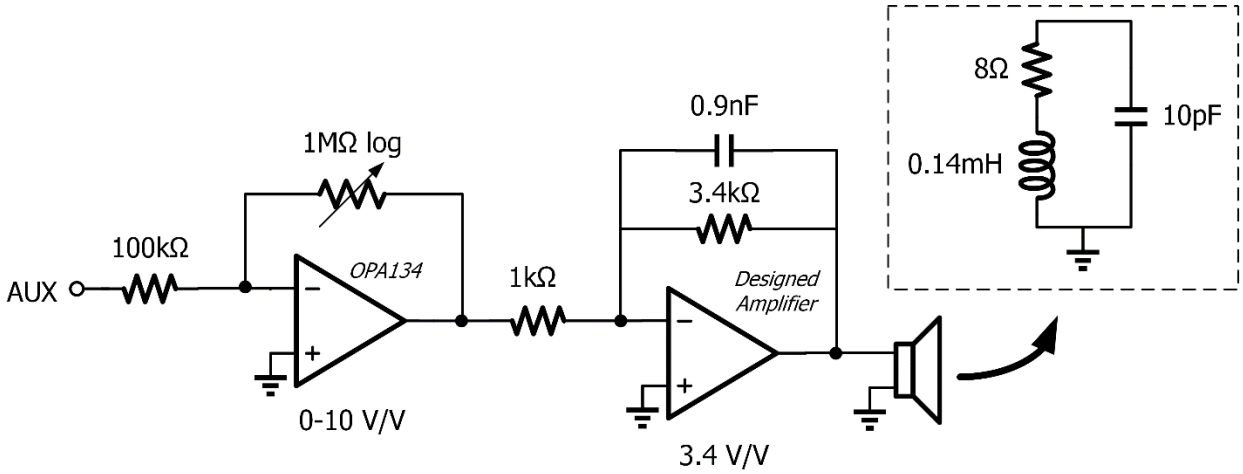

Figure 4: System block diagram

In the preamplification stage, a commercial amplifier, the OPA134, a low-noise and distortion audio opamp [4], is used in non-inverting configuration. In this stage, the gain is given by

$$\frac{V_o}{V_i}|_{Preamp} = -\frac{R_f}{100k\Omega}$$

where R_f is a log-scale potentiometer, with maximum value of 1MΩ. Figure 5 shows the characteristics of various scale potentiometers. Log scale is most advantageous for audio due to the slow increase in resistance. In the preamp, this means the gain is limited to less than unity for the first 50% of the potentiometer's rotation, allowing for fine tuning of volume below this level.

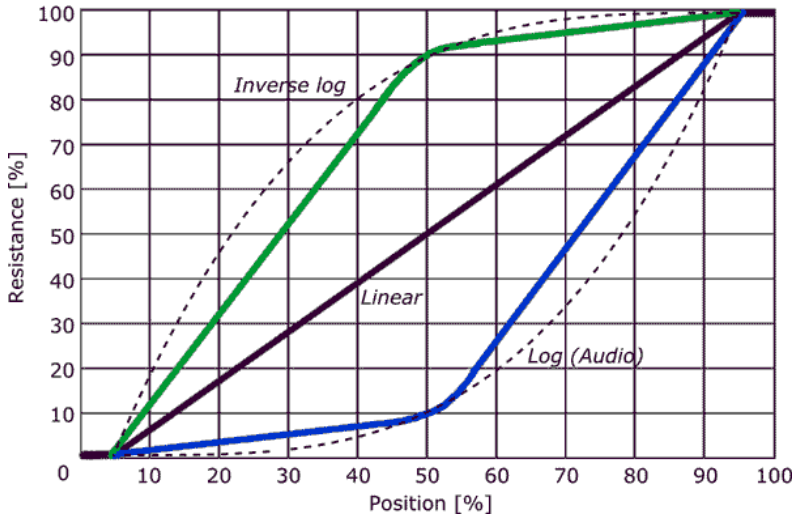

Figure 5: Potentiometer scale characteristics

In the second stage, a fixed gain is applied to the preamplifier output, and low-pass filtering is applied in order to limit the output bandwidth and thus noise. In inverting configuration, the gain is given as

$$\frac{V_o}{V_i}|_{Fixed} = -\frac{3.4k\Omega}{1k\Omega} = -3.4\ V/V$$

with a low-pass pole given by

$$f_{p1} = \frac{1}{2\pi R_f C_f} = \frac{1}{2\pi * 3.4k\Omega * 0.9nF} = 52kHz$$

A cutoff frequency of approximately 50kHz is selected to allow adequate bandwidth headroom to not attenuate any audio frequency components and achieve a flat response.

The speaker selected for this application is the Dayton Audio CE81PF-8. It is a 3" driver with maximum power of 15W and 8Ω impedance [5]. The speaker's frequency and impedance response are shown below in Figure 6/7.

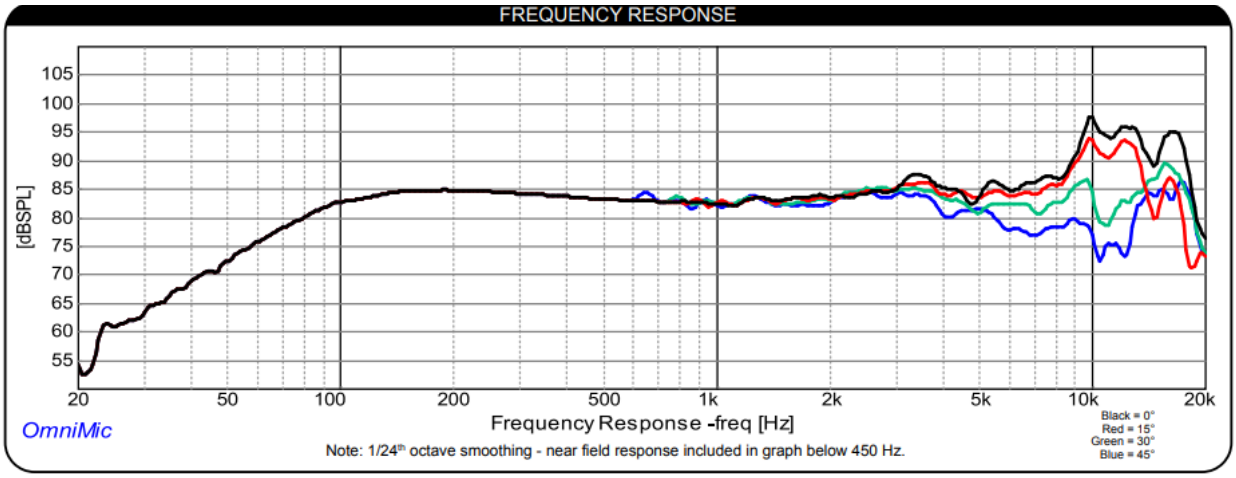

Figure 6: CE81PF-8 frequency response

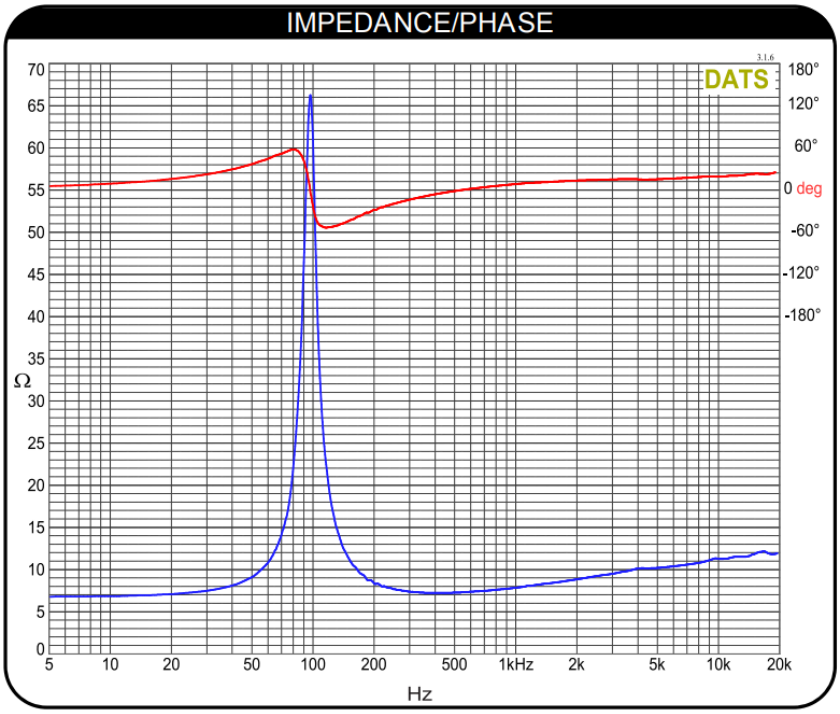

Figure 7: CE81PF-8 impedance and phase response

2.2. Core Amplifier Design

Next, an amplifier topology must be selected that is capable of producing >60dB of gain while allowing for an output swing of at least $10V_{pp}$. To achieve this, the bipolar 3 current mirror OTA is selected (Figure 8).

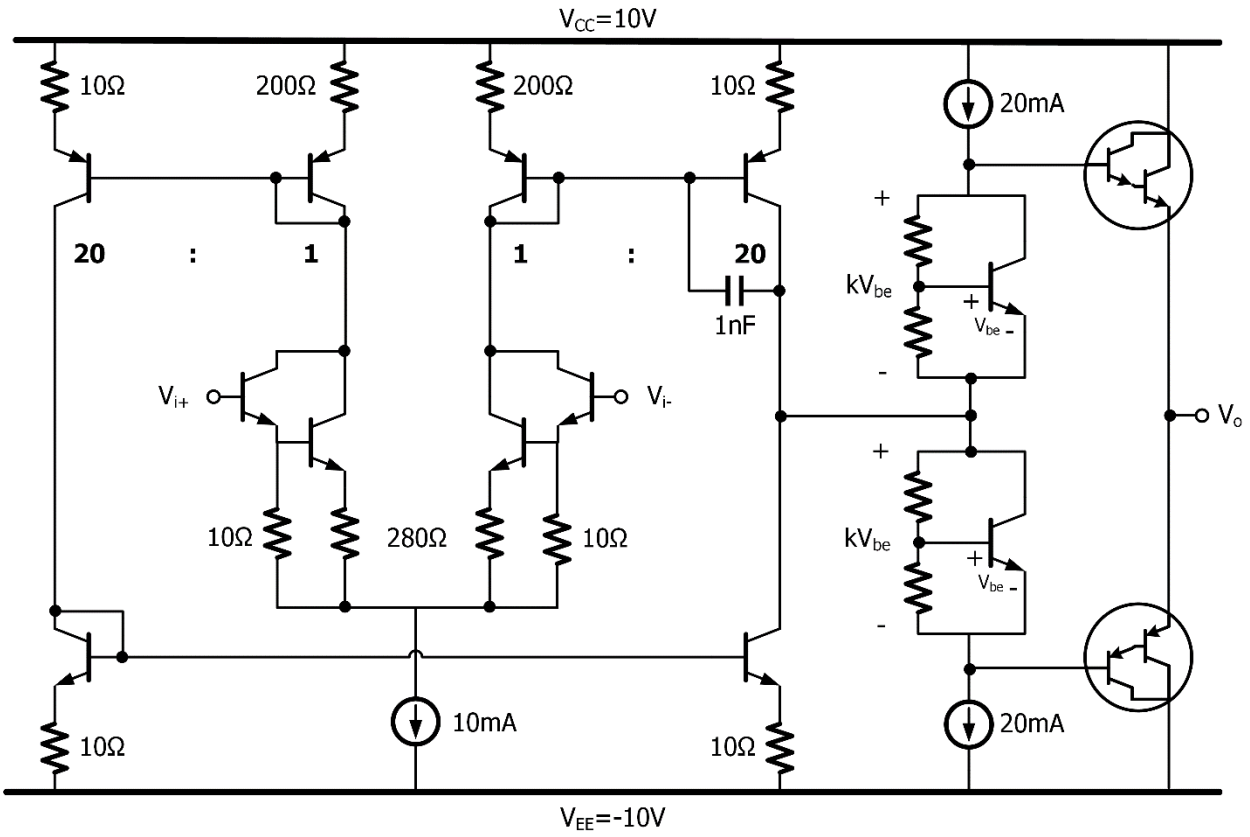

Figure 8: Core amplifier schematic

In the first stage, a common-emitter Darlington pair with degeneration is used. The gain of this stage is given by

$$\frac{V_o}{V_i} = \frac{-\alpha R_C}{r_e + R_E} \cong \frac{-R_C}{R_E}$$

While increasing the degeneration resistance increases linearity greatly, it does so at the cost of gain. By utilizing a Darlington pair, the value of alpha is maximized, and the emitter resistance is decreased. In addition, the input impedance of the Darlington pair is much higher than a single device, allowing for more ideal opamp operation.

From here, the signal is mirrored to the output, where the current mirror ratio is approximately given by the ratio of resistors. For this design, a ratio of 20:1 was selected to provide large gain. To ensure stability, a 1nF capacitor is placed across the output top current mirror. Small emitter resistance must be selected in order to allow for a large output swing.

For this stage, the small signal 2N3904 and 2N3906 transistors will be used [6][7].

2.3. Class-AB Output Stage Design

An output stage capable of driving the necessary current to the load at low distortion must be selected. For this, a class-AB emitter-follower topology is selected. To generate base voltage bias necessary for class-AB operation, the V_{BE} battery is used to allow for flexible biasing. A current bias of 20mA is supplied for the biasing circuitry. On the output, specialized Darlington pair power transistors are used. These devices must be capable of supplying the necessary current and dissipating considerable power. The output from the core amplifier must be DC coupled to eliminate any unwanted frequency effects. Thus, the output DC level must be set to approximately zero. Inverting feedback helps to achieve this.

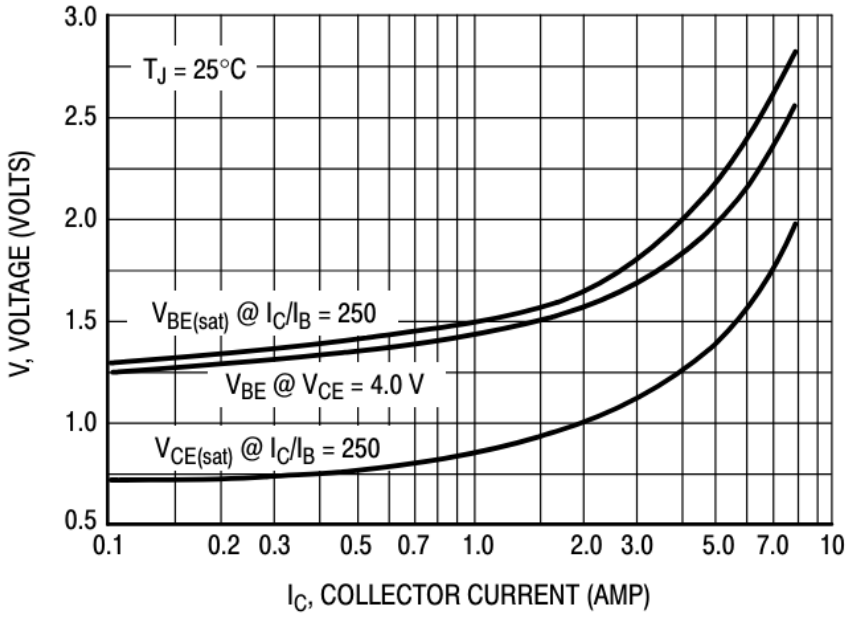

Figure 9: TIP122/127 on-voltage behavior

In this stage, the TIP122 and TIP127 transistors will be used [8]. These are Darlington pair power transistors, capable of delivering 5A and dissipating 65W with heatsinking. Figure 9 shows the cutoff behavior of the power BJTs. From this, a base voltage bias of around +/-1.4V was selected.

2.4. Current Source Design

To drive the above circuits, a current source must be designed. Since high output resistance is needed to avoid degradation of gain, the typical constant current drive cannot be used. Instead, the current mirror as shown in Figure 10 is used. With a mirroring ratio of 1:1 as shown, the output current generated is approximately equal to

$$I_O = \frac{V_{CC} - V_{EE} - V_{BE}}{R_C}$$

assuming low emitter resistors. The output resistance of the current mirror is then equal to

$$R_O = \frac{V_A}{I_{CE}}$$

where V_A is the early voltage, a device parameter. This output resistance is much higher than the effective resistance that would be needed for an equivalent bias current.

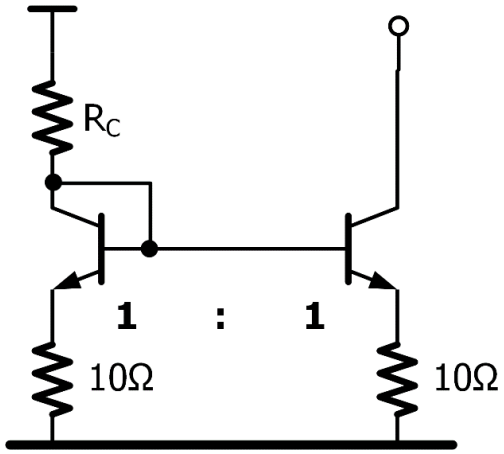

Figure 10: Current mirror schematic

3. Simulation Results

The system was first verified in Multisim using the relevant device models. The simulation results are summarized below in Table 2 and the relevant plots are included below.

Table 2: Simulation Result Summary

Specification	Desired	Simulated
Output Swing (max)	> 4.5V_{pk}	8V_{pk}
Output Power (max)	> 1W_{rms}	4W_{rms}
Open Loop Gain	> 60dB	62.58 dB
Phase Margin	> 45°	104°
CL Bandwidth	> 50 kHz	51.5 kHz
THD @ 1W_{RMS}	< 1%	0.035%
THD @ 4W_{RMS}	---	0.748%
THD @ 0.1W_{RMS}	---	0.00284%
Quiescent Power	---	4.3W
Input-Referred Noise	---	8.52µV_{RMS}

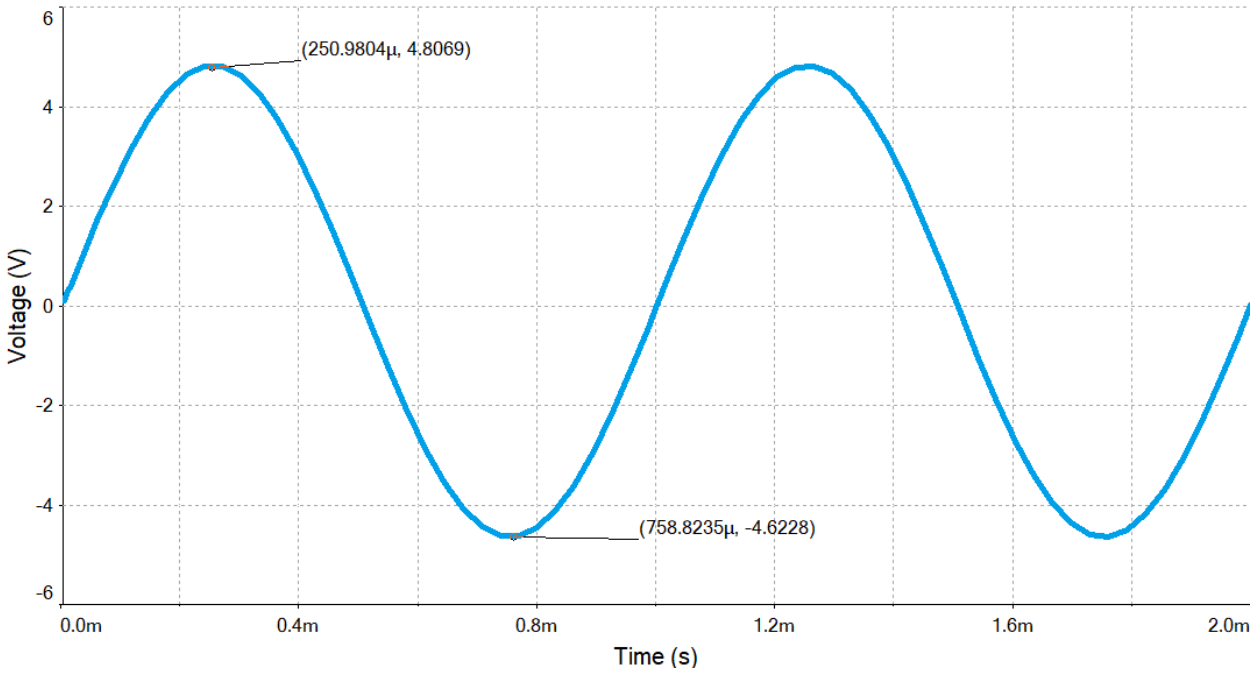

Figure 11: Output voltage swing @ 1W_{RMS} output

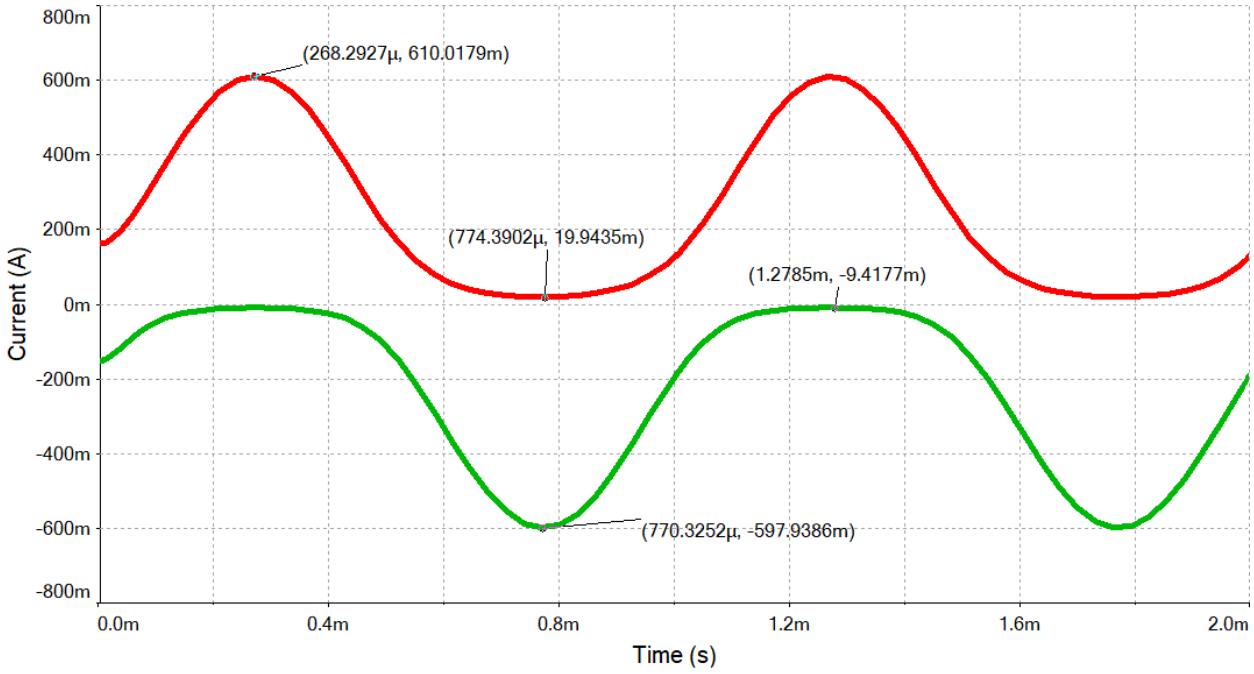

Figure 12: Output device currents @ $1W_{RMS}$ output

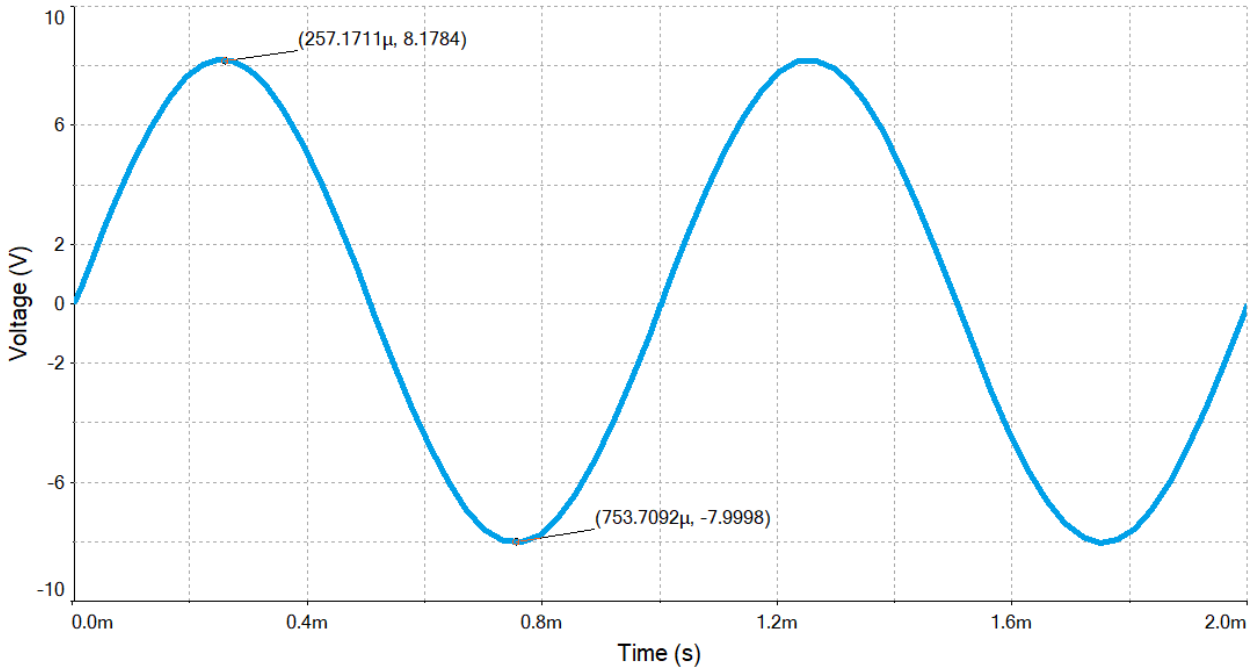

Figure 13: Output voltage swing @ $4W_{RMS}$ output

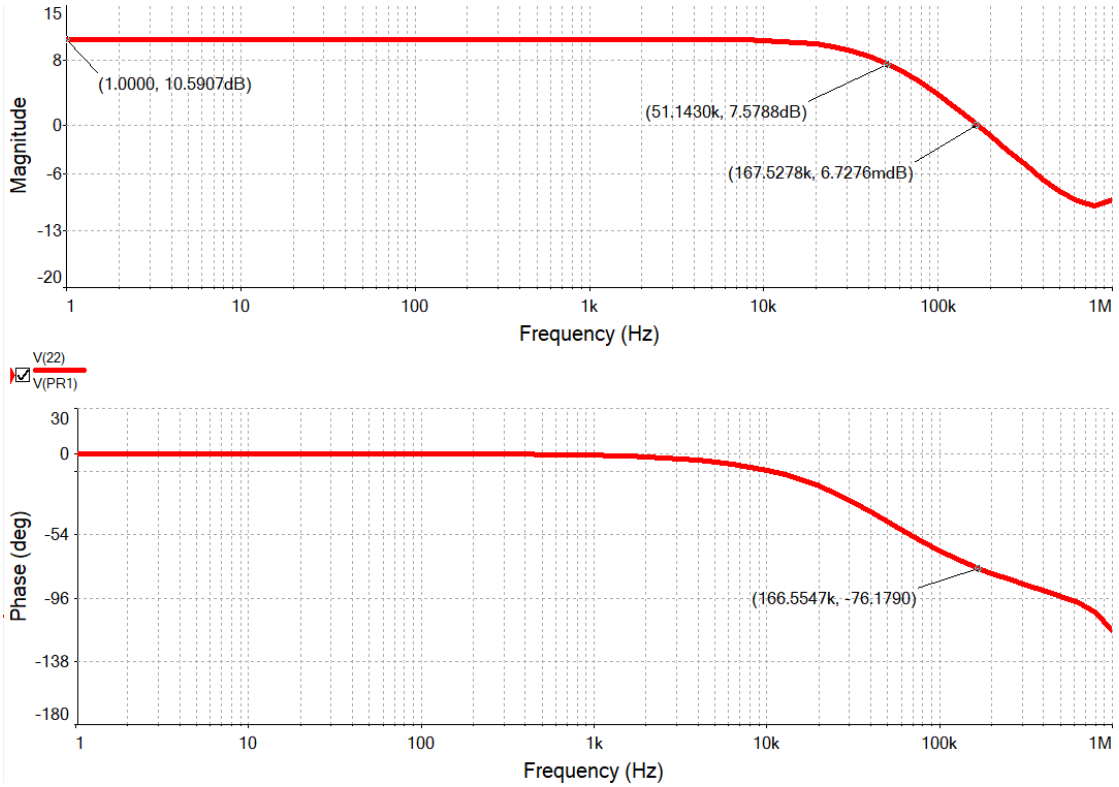

Figure 14: Closed loop AC response

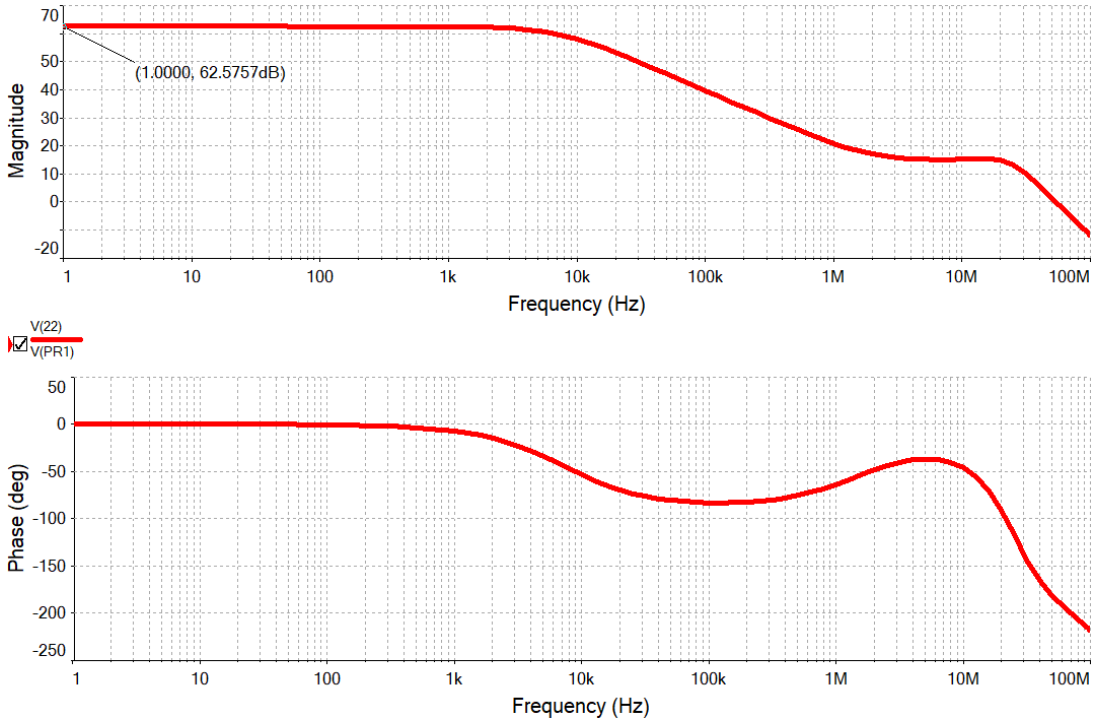

Figure 15: Open loop AC response

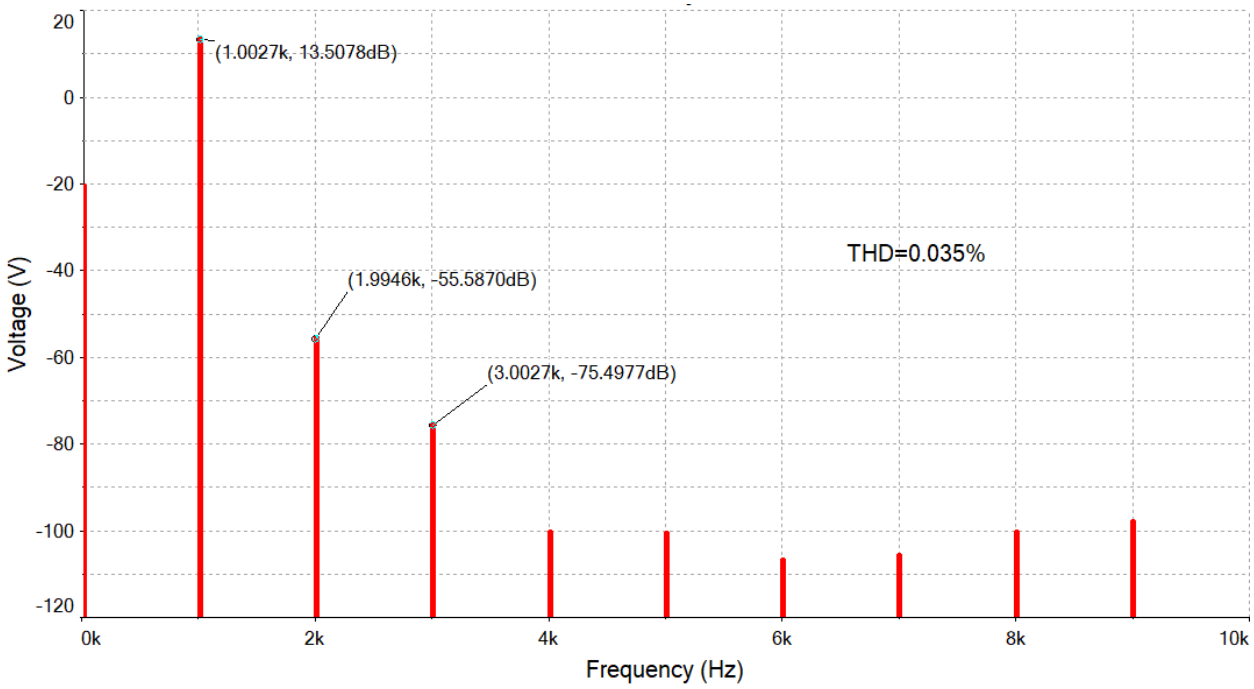

Figure 16: Spectrum for 1kHz input @ $1W_{RMS}$ output

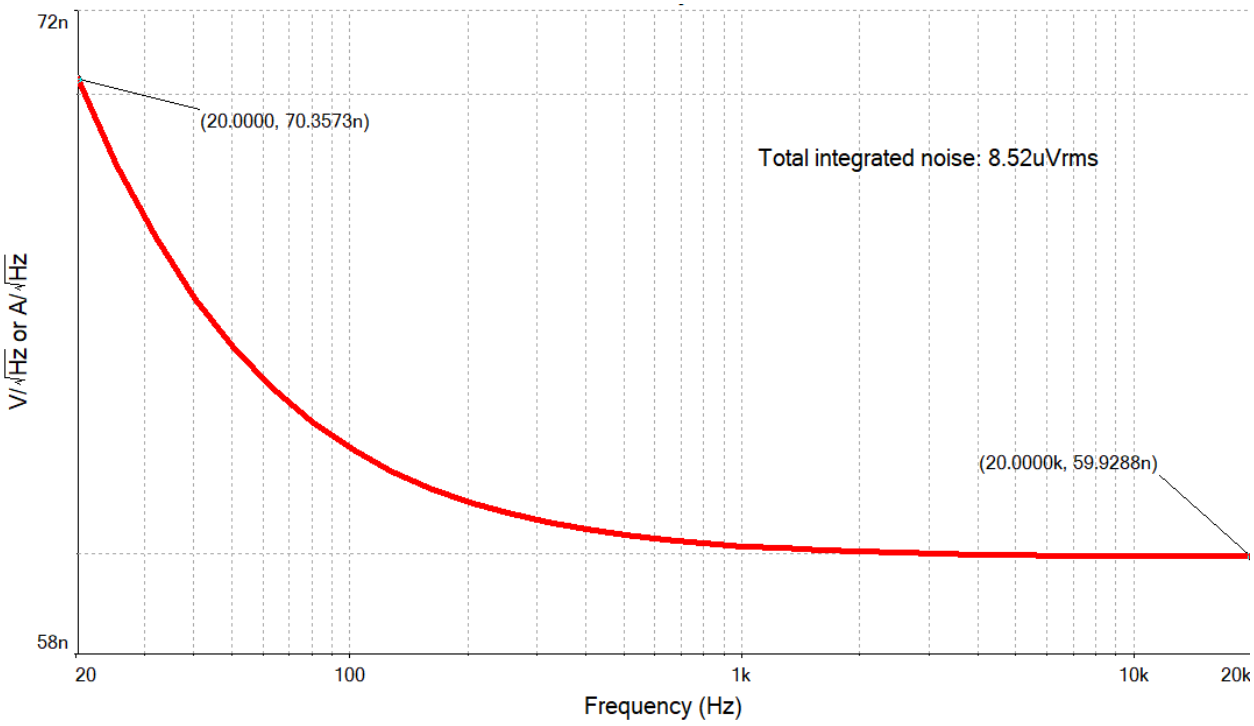

Figure 17: Input-referred noise density

4. Experimental Results

To test the amplifier, the circuit was assembled on a breadboard with discrete components. In order to ensure thermal failure does not occur, some devices were placed in parallel as shown in Figure 18. By utilizing this configuration, the current is split evenly four ways, thus each device dissipates one quarter of the power the single device would.

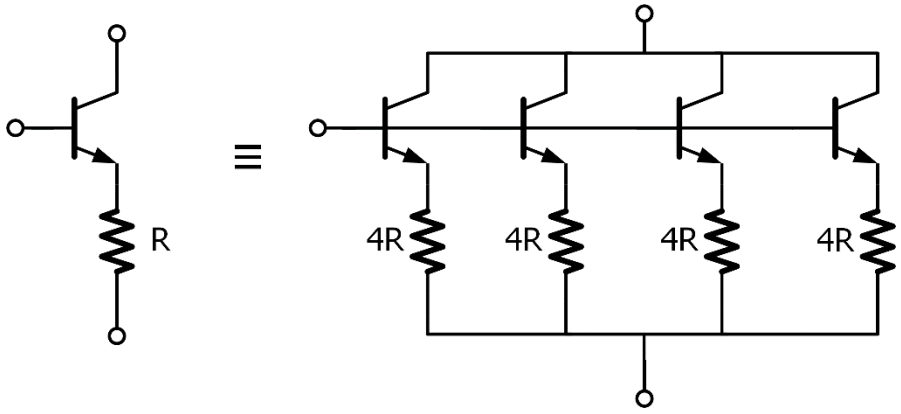

Figure 18: Parallel connection scheme for high-current devices

The test setup is shown in Figure 19. The OTA and output stage were assembled on separate breadboards to reduce thermal coupling as much as possible and assist in ease of measurement. The Analog Discovery 2 device was used to take measurements and generate the necessary waveforms. The achieved results are summarized in Table 3. Due to breadboard thermal limitations, the highest swing tested was around $3.6V_{pk}$. Due to AD2 noise and flywire capacitive coupling, a significant noise floor was observed in the spectrum measurements, yielding the THD measurements inaccurate. Nevertheless, the waveforms appear quite linear, and no significantly higher harmonics are observed above the noise floor in the spectrum. The noise floor is around -40dB.

Table 3: Measurement Result Summary

Specification	Simulated	Measured
Output Swing (max)	$8V_{pk}$	$3.6V_{pk}$
Output Power (max)	$4W_{rms}$	$0.8W_{rms}$
Open Loop Gain	62.58 dB	36.7 dB
Phase Margin	104°	---
CL Bandwidth	51.5 kHz	67.2 kHz
THD @ $1W_{RMS}$	0.029%	3.864%
THD @ $4W_{RMS}$	0.748%	---
THD @ $0.1W_{RMS}$	0.00284%	---
Quiescent Power	4.3W	---

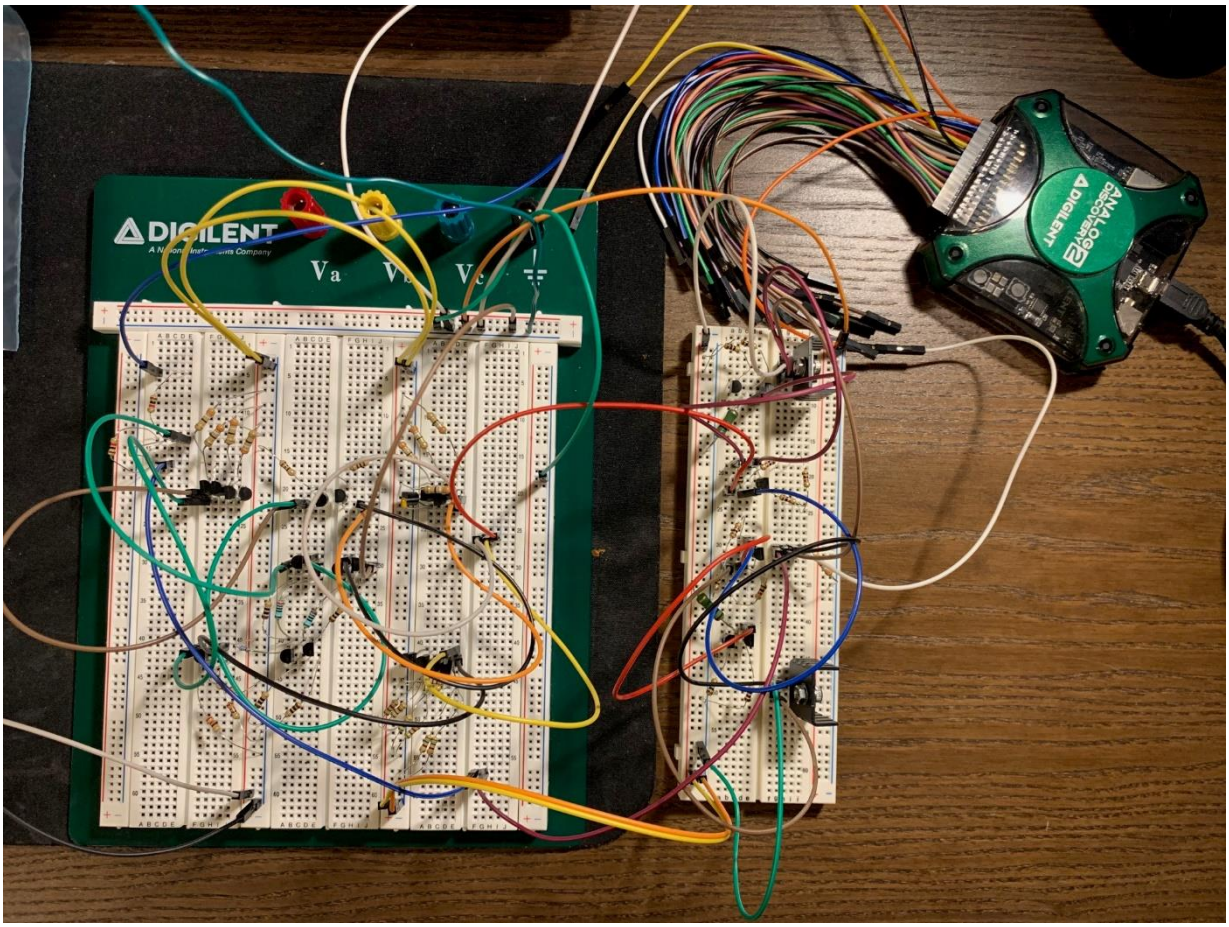

Figure 19: Test setup

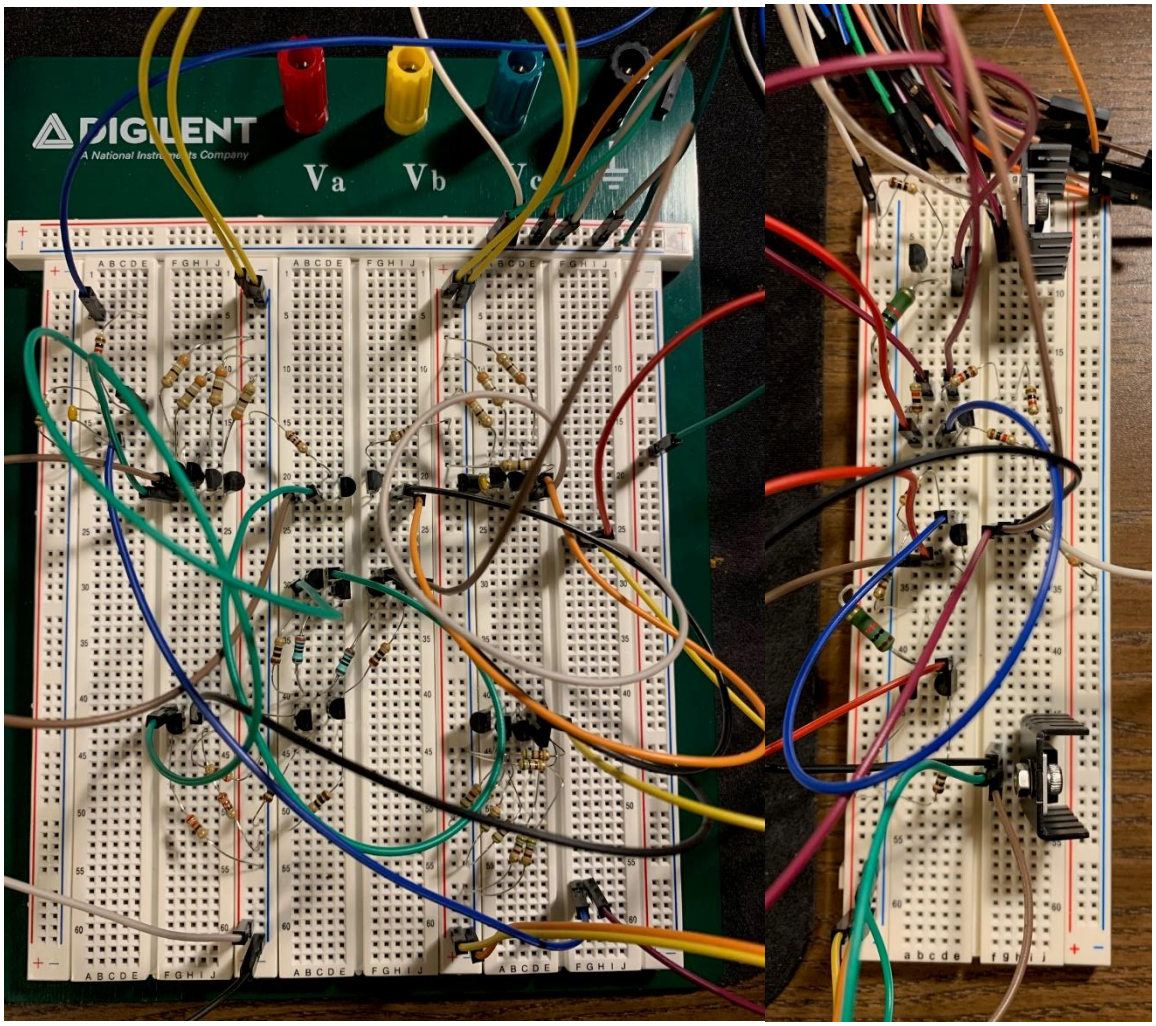

Figure 20: OTA (left) and output stage (right)

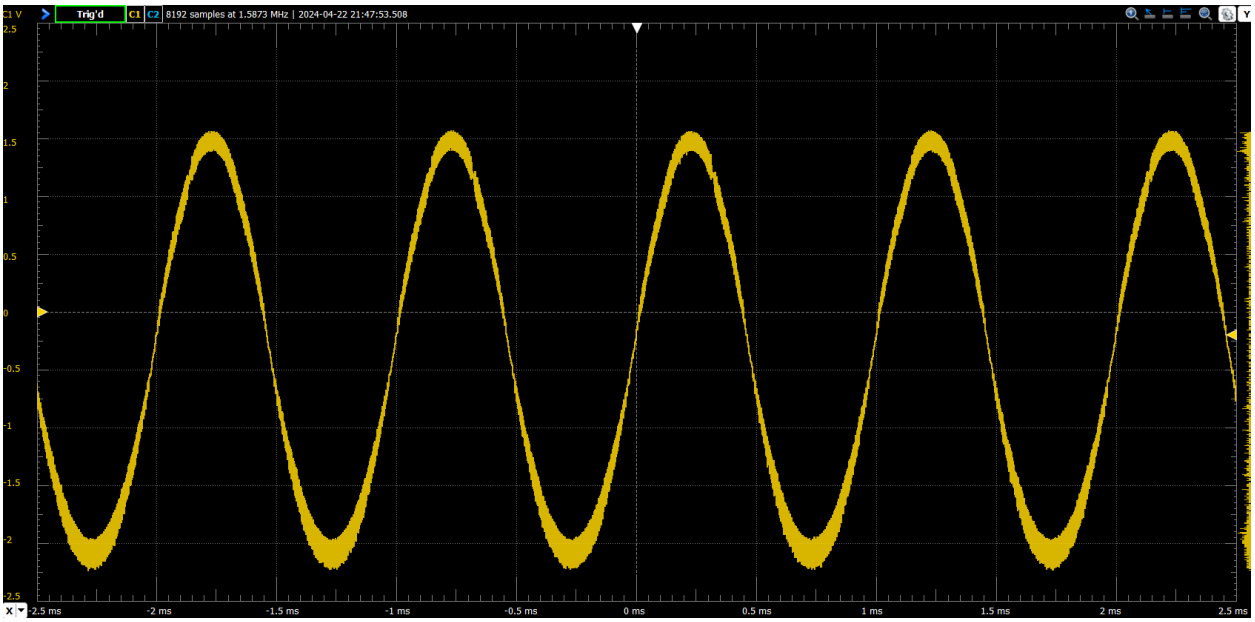

Figure 21: Output voltage swing @ 0.25W_{RMS} output

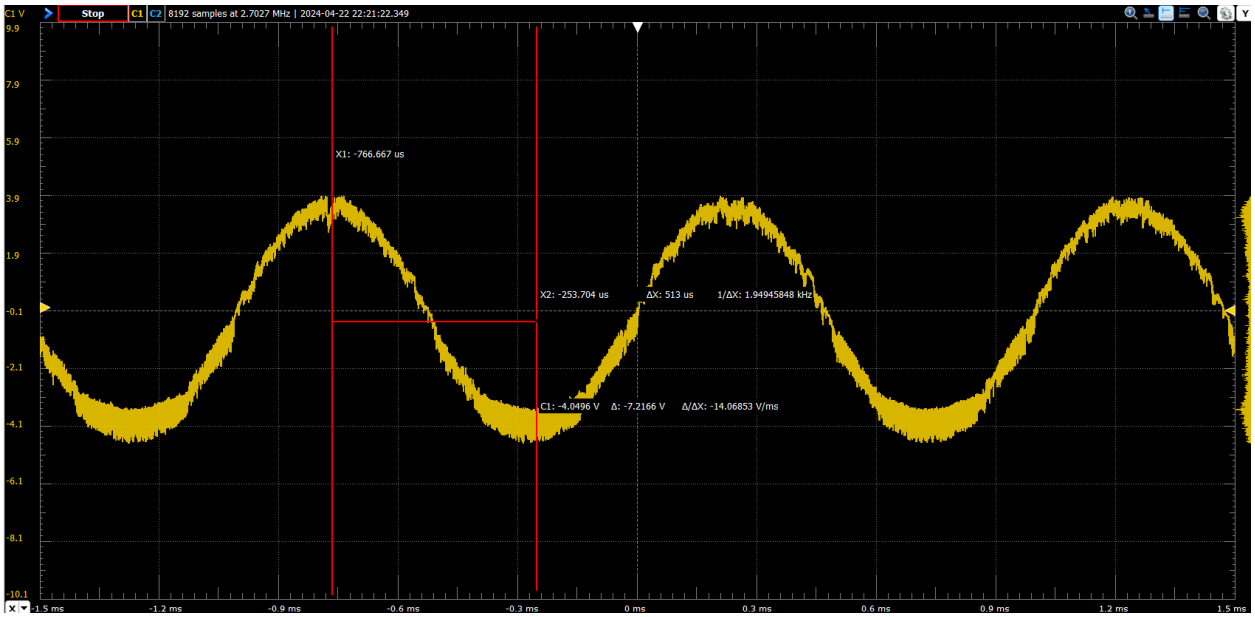

Figure 22: Output voltage swing @ 0.8W_{RMS} output

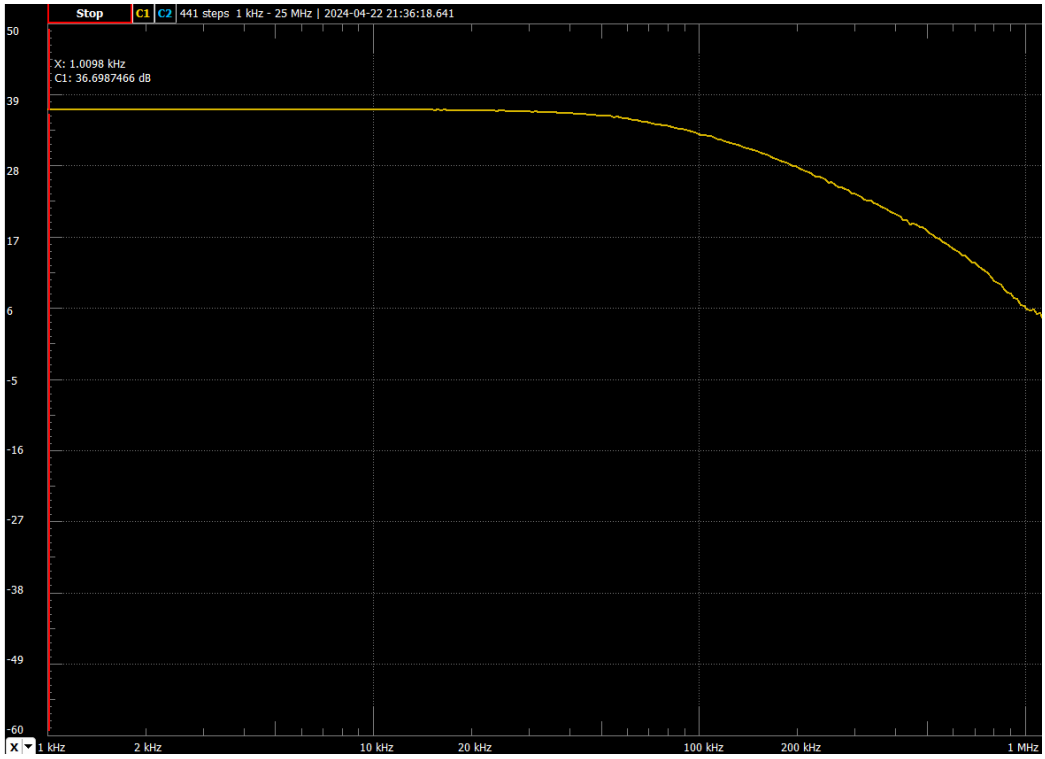

Figure 23: Open loop AC response

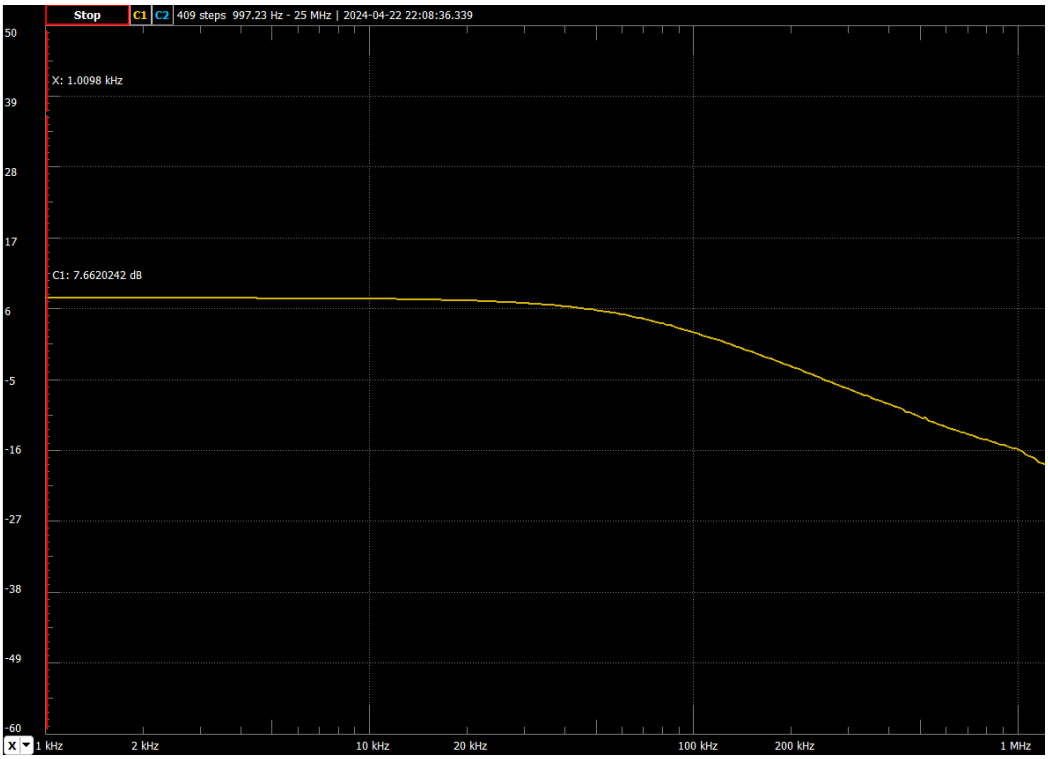

Figure 24: Closed loop AC response

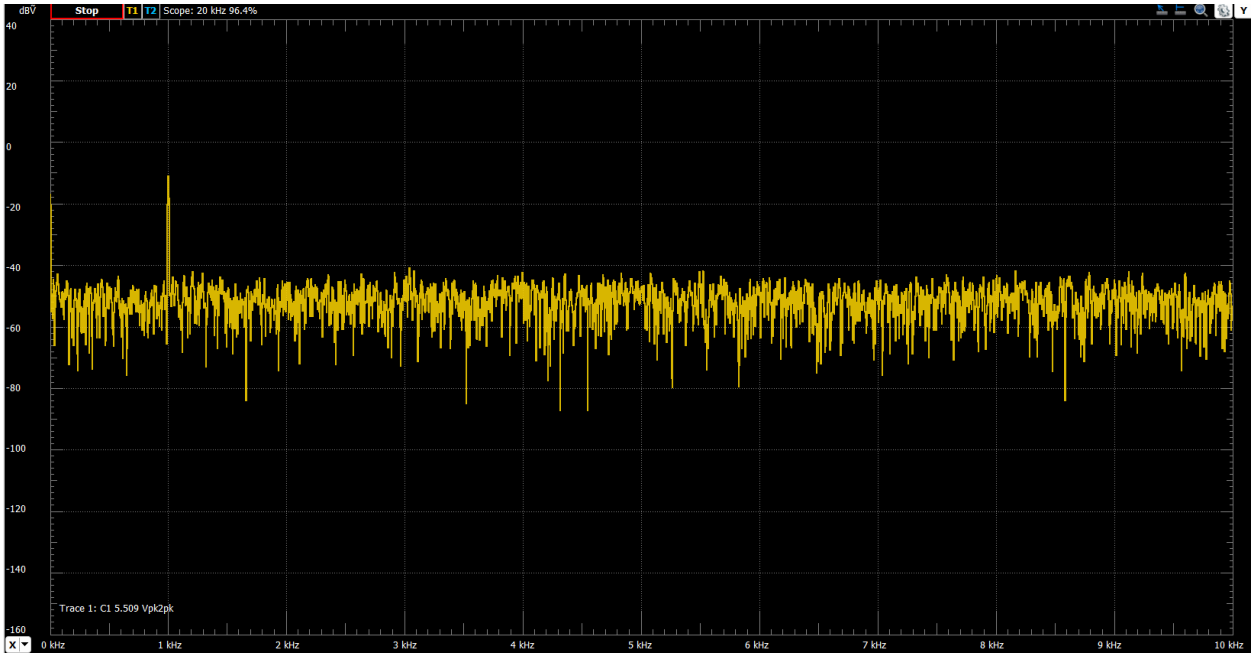

Figure 25: Spectrum for 1kHz input @ 0.8W_{RMS} output

4.1. Auditory Test

Finally, the system was verified with the speaker attached and an audio signal input. The test setup is shown in Figure 26. A line-level RCA input is taken from a commercial DAC and input into the preamp stage of the circuit. The speaker is attached to the output and the volume is modulated using the potentiometer in the preamp stage.

Overall, the audio quality was very good, with some white noise present, as is apparent in the spectrum measurement of Figure 25. This is likely due to both thermal noise in the output transistors and non-idealities associated with the breadboard, flywires, and overall test setup. The output volume increases with the potentiometer as desired, only clipping at high levels of volume when the input range of the core amplifier is exceeded.

As expected, the volume levels remain relatively constant over supply voltage variation, displaying higher distortion and lower linearity at lower supply voltages, when the output stage is operating more as a class-B amplifier. At nominal supply levels or even slightly lower, the distortion and linearity is far improved, with a much cleaner sounding output signal. As the output transistors heated up, the power consumption increased, and the signal distortion also increased. This likely means that the transistors are heating up very close to their maximum tolerable temperature.

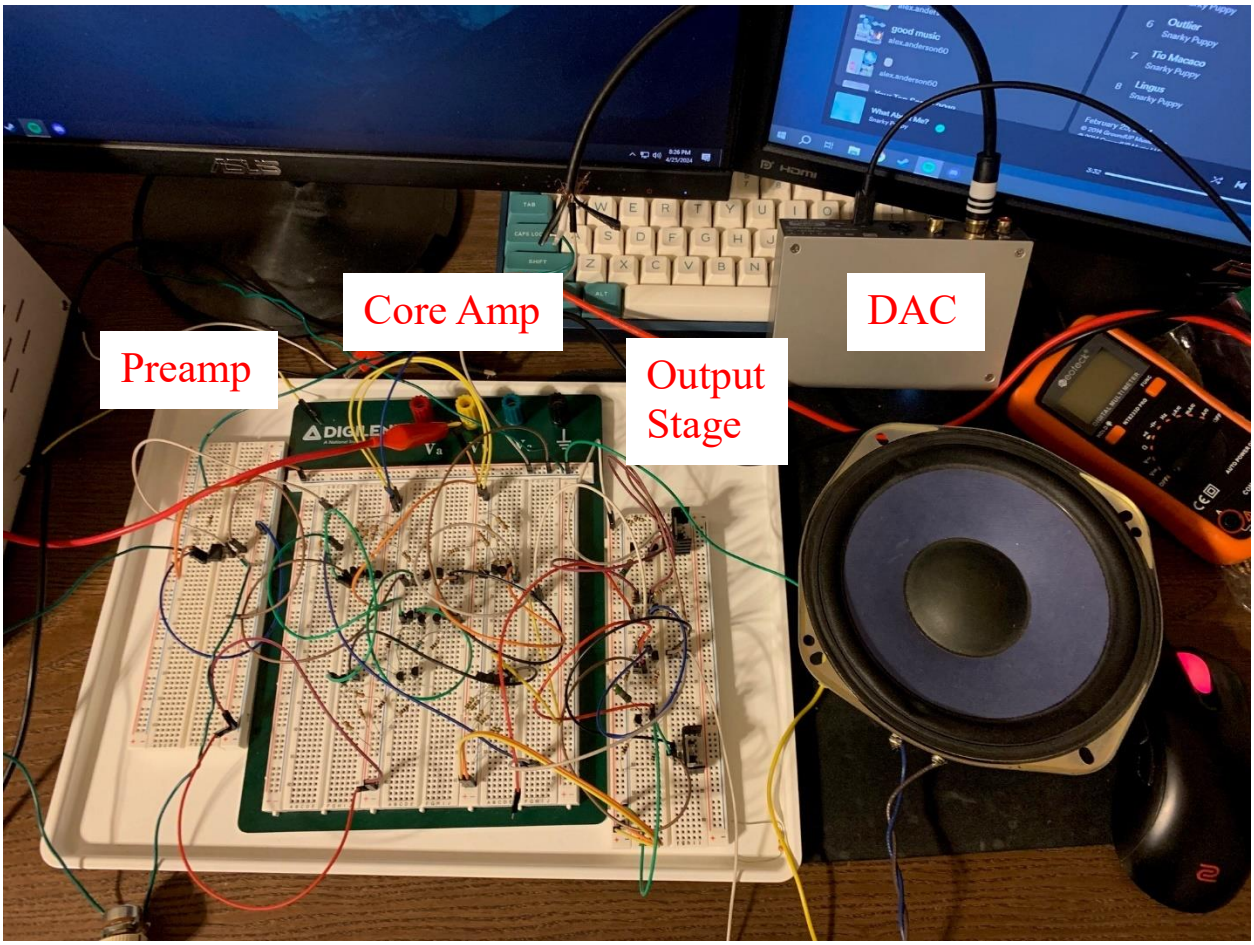

Figure 26: Audio test setup

5. Conclusion

In this report, the design of a class-AB audio amplifier was discussed, and simulation and measurement results were presented. Results were slightly worse in measurement compared to simulation. This can almost certainly be attributed to test setup and higher order effects such as capacitive coupling, crosstalk, noise, and component variation. Particularly, the breadboard is not ideal for high-power applications such as this, as the performance is deteriorated at high levels of current, leading to performance variations and at worse, device failure.

With more time, one could integrate the circuit on a perfboard or PCB, eliminating many of the issues associated with the breadboard setup. In addition, better measurement equipment would allow more accurate characterization of the system. Nevertheless, the concept of the class-AB amplifier was successfully demonstrated in practice, with the output transients displaying good linearity performance.

In practice, with the attached speaker, the audio quality was good. Some noise was present, probably due to the non-ideal test setup.

6. References

[1] Sidney, D. (1953). Semiconductor Signal translating device (Patent No. US2663806A). U.S. Patent and Trademark Office.

[2] R. Hogervorst, J. P. Tero, R. G. H. Eschauzier and J. H. Huijsing, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," in IEEE Journal of Solid-State Circuits, vol. 29, no. 12, pp. 1505-1513, Dec. 1994, doi: 10.1109/4.340424.

[3] J. Beloso-Legarra, C. A. de La Cruz-Blas and A. J. Lopez-Martin, "Single-Stage Class-AB Non-Linear Current Mirror OTA," 2022 37th Conference on Design of Circuits and Integrated Circuits (DCIS), Pamplona, Spain, 2022, pp. 1-6, doi: 10.1109/DCIS55711.2022.9970198.

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[6] Onsemi, “General Purpose Transistors NPN Silicon 2N3903, 2N3904,” 2N3903/D, Aug. 2021.

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