A 2.4-GHz Direct-Conversion Merged LNA-Mixer and QVCO in 90nm CMOS

Alex Anderson and Chaw Chuen Ng (Mike)
UIN: 728001757 and 33200800
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***Abstract*—This report discusses the design and simulation of a 2.4GHz direct-conversion frontend in 90nm CMOS. The design utilizes a fully differential merged LNA-mixer and the corresponding 2.4GHz quadrature VCO. All inductors were implemented in EM simulation and are included in the final results. The design achieves a conversion gain of 28dB with a noise figure of 5.3dB at IF, and an input-referred IP3 of 0.3dBm. The entire frontend dissipates 9.2mW.**

I. Introduction

In RF system design, various receiver architecture choices exist, including the heterodyne, direct-conversion, and image reject architectures, each offering advantages and disadvantages with respect to complexity, image rejection, and channel selection. Depending on the desired application, receiver choice must be selected with regard to system specifications such as total gain, noise figure, and linearity. Additionally, receiver systems often operate in environments requiring low power consumption such as cell phones, watches, and laptops. Thus, efficient circuits are required on the front-end to reduce the required system power, prompting the use of "merged" circuits, where the power is minimized greatly.

The 2.4GHz band carries a wide variety of standards, including Wi-Fi (IEEE 802.11), Bluetooth (IEEE 802.15.1), and many other device types including car alarms, radars, and AV systems. Thus, strict separation of bands is crucial to prevent interference. On a system level, this has two primary implications: band selection must have sharp cutoffs, and the image generated during downconversion in the mixer must not cause interference in other nearby bands. One solution to both of these problems is the use of a direct-conversion topology.

II. Background

A. Direct-Conversion Receivers

Fig. 1 shows a typical direct-conversion receiver frontend [1]. In receivers, the down-converted frequency is given as

$$f_{IF} = f_{LO} - f_{in} \tag{1}$$

In direct-conversion receivers, the LO frequency is chosen extremely close to the input RF frequency, yielding an IF relatively close to DC.

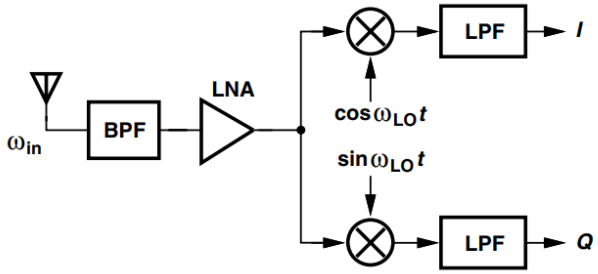

Fig. 1. Direct-conversion receiver frontend.

The direct-conversion or zero-IF receiver architecture converts the incoming RF signal directly to baseband in the first downconversion, eliminating the image present in the heterodyne receiver. Additionally, since the IF is at very low frequency, often below 10MHz, a simple lowpass filter can be used for channel selection, in contrast to the high-order bandpass filter typically used. High quality lowpass filters are far easier to implement on chip, allowing for more compact system integration.

Despite these upsides, some tradeoffs do exist. If the RF signal is asymmetrically modulated, self-corruption will occur. To solve this, the signal must be downconverted in separate phases, prompting the need for a quadrature LO. Additionally, since the LO frequency is very close to the RF input, the potential for interference appears through LO leakage to the antenna.

Since power consumption is often crucial in RF systems, the usage of "merged" LNA-mixer systems is advantageous in this regard. In a typical merged LNA-mixer, the amplified current generated through the LNA is fed directly through the mixer, in a cascode way, in contrast to the typical cascaded LNA-mixer architecture. The major downfall of this topology is linearity, especially when the mixer supply voltage is relatively low compared to the device threshold voltages. With many devices stacked up in this topology, the IIP3 and gain compression point decrease significantly and are directly limited by the overdrive voltages of the devices. – a function of process threshold voltage. Thus, in modern CMOS processes with low supply voltages relative to the threshold voltages, IIP3 must be sacrificed for low noise figure and power. Despite the linearity limitations, the merged architecture allows for excellent noise and gain performance.

III. Proposed Circuit

In this section, the proposed topology is presented, and the design considerations are discussed.

A. Conceptual Idea

On a high level, the merged LNA-mixer has two parts: a gain stage and a mixing stage. The gain stage is a simple cascode common-source LNA, with gate and source inductors for input matching (*Fig. 2*). Additionally, a fixed capacitance is introduced from the gate to source of the input transistor in order to decouple the input quality factor from the noise figure of the circuit [2]. The mixer part is the top of a Gilbert cell quadrature mixer, with the LNA acting as the RF input transistors, generating the signal current to be steered (*Fig. 3*).

B. LNA Design

For the LNA part of the circuit, the standard common-source cascode LNA is selected for its high gain and ease of input matching. The input matching procedure is described below.

Referring to the components in Figure 2, from [3], ignoring C_{gd} and g_{mb} the input impedance is,

$$Z_{in} = \frac{1}{j\omega\left(C_D+C_{gs_{M1}}\right)} + j\omega(L_G + L_S) + g_{m_{M1}}\frac{L_S}{\left(C_D+C_{gs_{M1}}\right)} \quad (2)$$

The resonant angular frequency is,

$$\omega_O = \frac{1}{\sqrt{(L_G+L_S)\left(C_D+C_{gs_{M1}}\right)}} \quad (3)$$

For impedance matching, where the source impedance is represented as R_s, ideally at 50Ω, the equation can be expressed as,

$$R_s = g_m\frac{L_S}{\left(C_D+C_{gs_{M1}}\right)} \quad (4)$$

The quality factor Q of the input circuit is then,

$$Q = \frac{1}{\left(R_S+g_m\frac{L_S}{C_D+C_{gs_{M1}}}\right)} = \frac{1}{2R_S\omega_O} \quad (5)$$

Using these equations, values for L_G, L_S, and C_D were selected to be 12nH, 100pH, and 250fF respectively.

The width of the input transistors can be determined using the g_m/I_D methodology [4], whereas the peak transit frequency is chosen for a given overdrive voltage, which is determined from the desired IIP3 specification. With a common-mode voltage of 650mV, aspect ratios of M1 and M2 are chosen to be (80/0.1) and (70/0.1) micron respectively.

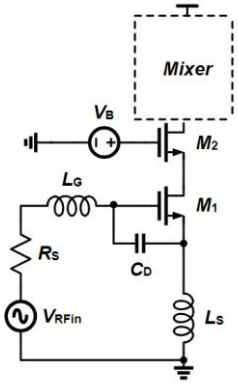

Fig. 2. LNA portion of receiver.

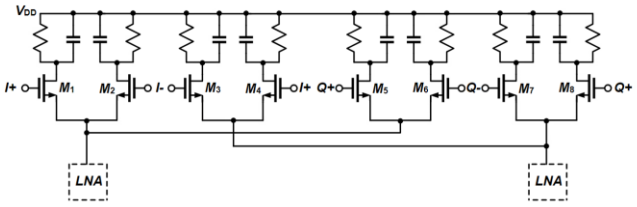

Fig. 3. Mixer portion of receiver.

C. Mixer Design

The mixer topology chosen is the standard Gilbert cell with quadrature inputs to implement the necessary phase separation for direct-conversion receivers. Similar to the LNA, the DC voltage at the gate of the switching transistors can be determined from the linearity restriction and was chosen to be 700mV. The aspect ratio of the input transistors produces a tradeoff between gain and linearity performance, but a good balance was a value of (125/0.2) micron. The use of load resistors delivers excellent gain but consumes valuable DC headroom for large values. Thus, a load resistance of 400Ω was chosen, with a capacitance of 1.5pF. Finally, the choice of LO amplitude remains, and is driven primarily by desired gain. In order to not force the switching transistors into the triode region, sacrificing linearity performance, a LO differential amplitude of 300mV was used.

D. Quadrature Voltage-Controlled Oscillator (QVCO)

In order to implement the quadrature down conversion necessary for the direct conversion receiver, a quadrature VCO is implemented using standard anti-phase coupling (*Fig. 4*). A coupling factor of α=0.6 was chosen. For low phase noise, a high-quality factor tank operating close to the ideal resonance is needed. To compensate for the output frequency shift due to antiphase coupling, degeneration inductors are added to shift the frequency closer to the resonance, improving phase noise performance significantly. A bias current of 1.2mA is selected along with a cross-coupled pair aspect ratio of (180/0.1) to provide optimal phase noise performance at relatively low power consumption. Standard MOS varactors are used to implement frequency control. Varactor sizes of (10/10) microns are used for a wide tuning range.

Realistic inductors were implemented in Sonnet (*Fig. 5*). The tank inductance is 2.5nH with Q-factor=18 at 2.4GHz, and the degeneration inductance is 4.4nH with Q-factor=14 at 2.4GHz.

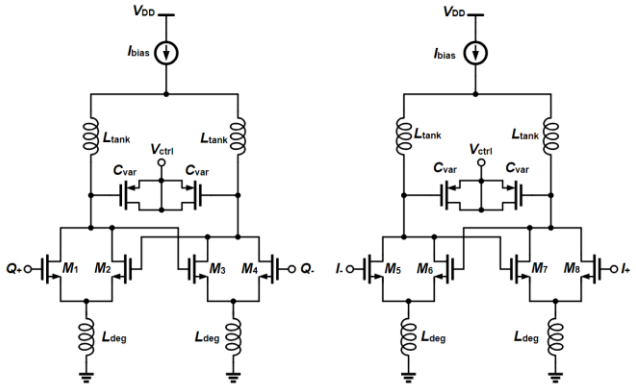

Fig. 4. Quadrature VCO schematic.

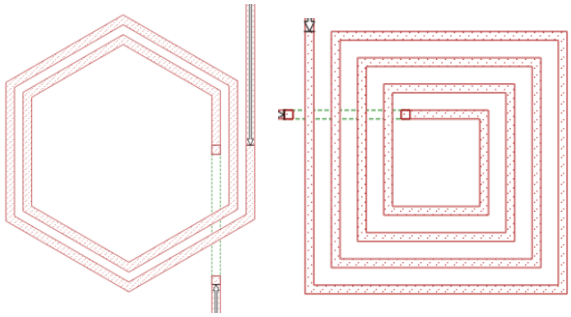

Fig. 5. QVCO inductors: tank (left), degeneration (right).

IV. Results

In this section, the QVCO and overall system performance is presented, and relevant plots are shown.

A. QVCO Results and Comparison

The QVCO results are summarized in Table I. Overall, the design gives excellent phase noise performance at an extremely low power and a tuning range is +/-12%.

TABLE I. Comparison of QVCOs

Reference	Tuning Range [GHz]	Phase Noise @ 1MHz Offset [dBc/Hz]	Power [mW]
This work	2.12 – 2.75	-122.9	2.88
[5]	1.67 – 1.97	-132	50
[6]	1.71 – 1.99	-138	20
[7]	1.05 – 1.39	-120	5.4
[8]	2.40 – 2.64	-110.5	14.4

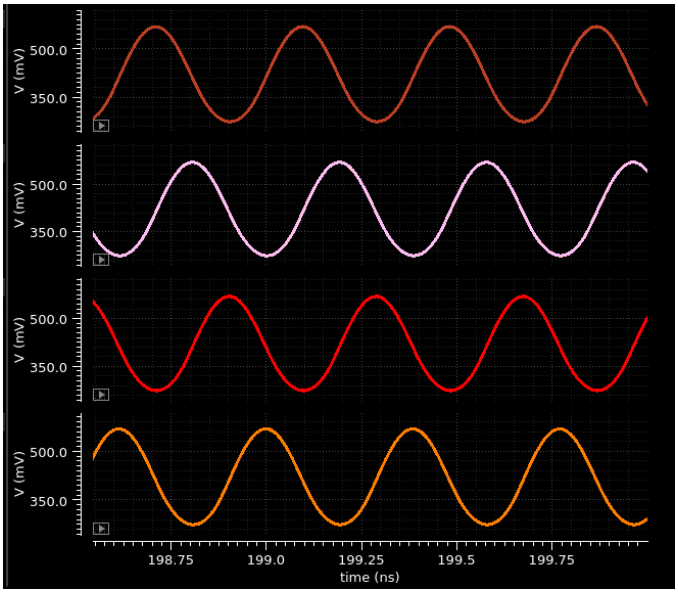

Figure 6: QVCO outputs. From top to bottom: I+, Q+, I-, Q-

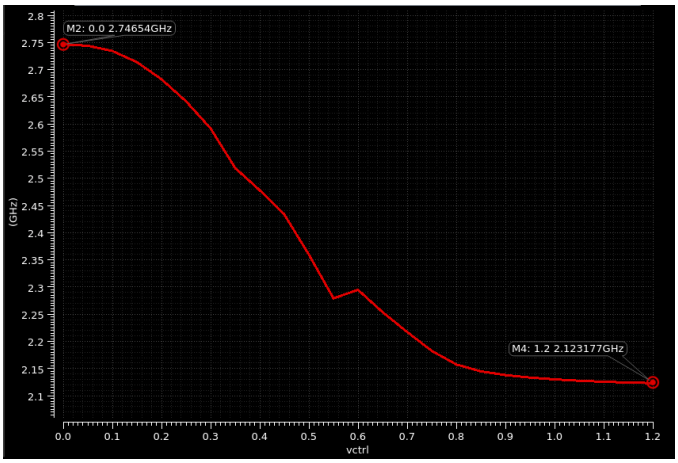

Figure 7: QVCO tuning range.

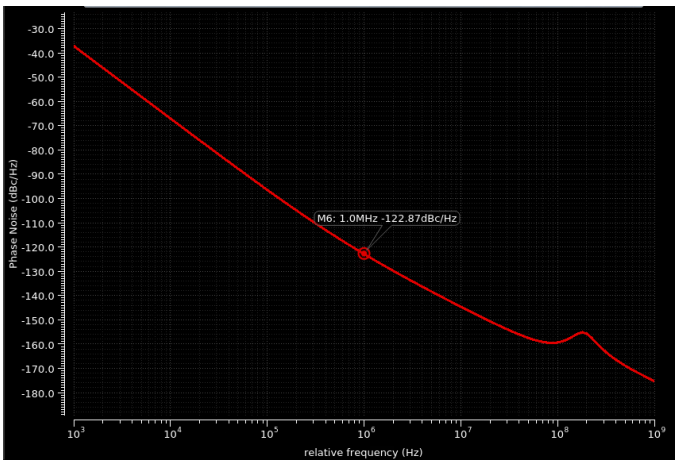

Figure 8: QVCO phase noise vs. offset frequency.

B. *LNA-Mixer Results with Realistic Inductors*

Once the ideal Q-factor and L were identified to meet the NF, Gain, IIP3, and S_{11} specifications, realistic inductors were implemented. In the LNA, L_S was implemented with an inductance of 114pH and Q-factor of 10 at 2.4GHz. The initial estimation of inductor dimensions is done using [9]. The inductor L_G was also implemented as 12.3nH with a Q-factor of 11.8 at 2.4GHz. As mentioned in [10], the inductance value of tens of nH magnitude and a high Q-factor is difficult to achieve using an on-chip inductor process due to the huge area. On top of that, the inherent parasitic resistance of a monolithic inductor results in a low Q-factor value.

$$Q = \frac{\omega L}{R} \tag{6}$$

Thus, the more realistic approach would be to implement L_G off-chip. The inductor has still been laid-out in this project in Sonnet, but the practicality is something that needs to be revisited if a real RFIC is intended to be fabricated. With a well designed off-chip inductor, the noise figure can certainly be reduced to less than 5dB.

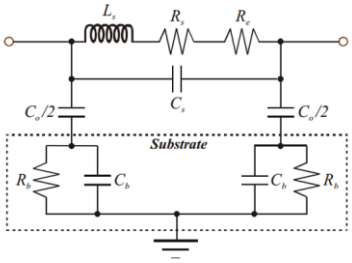

Fig. 9. Circuit-level characterization of the monolithic inductor. [10]

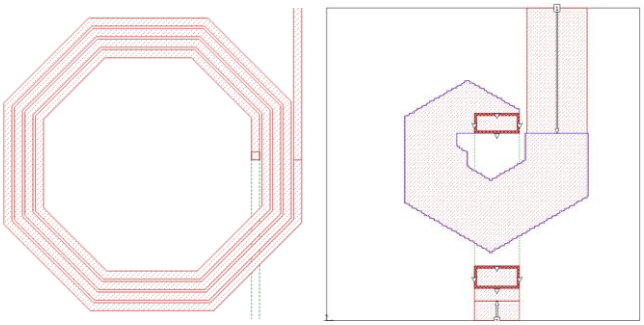

Fig. 10. LNA inductors - L_G (left) and L_D (right)

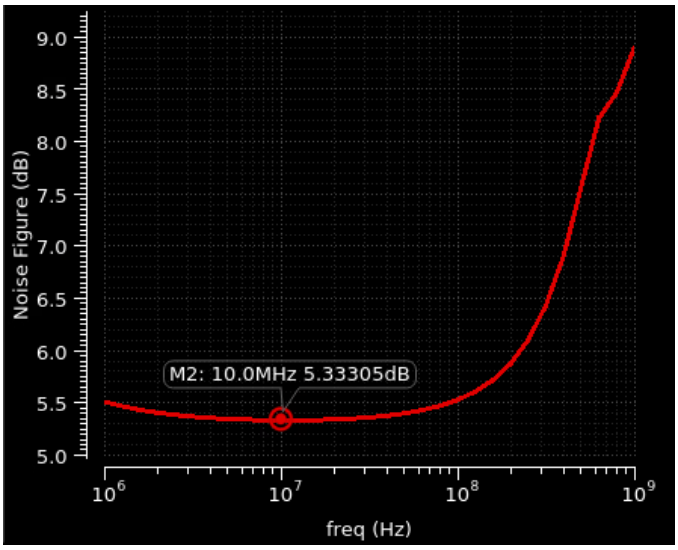

Fig. 11. Noise figure with realistic inductor.

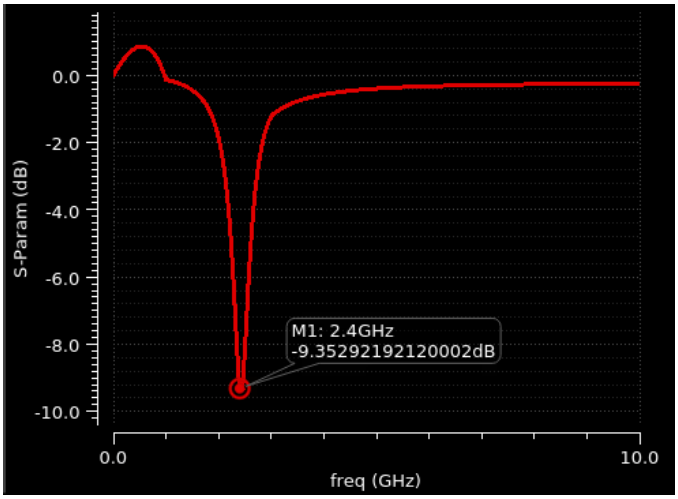

Fig. 12. S_{11} with realistic inductor.

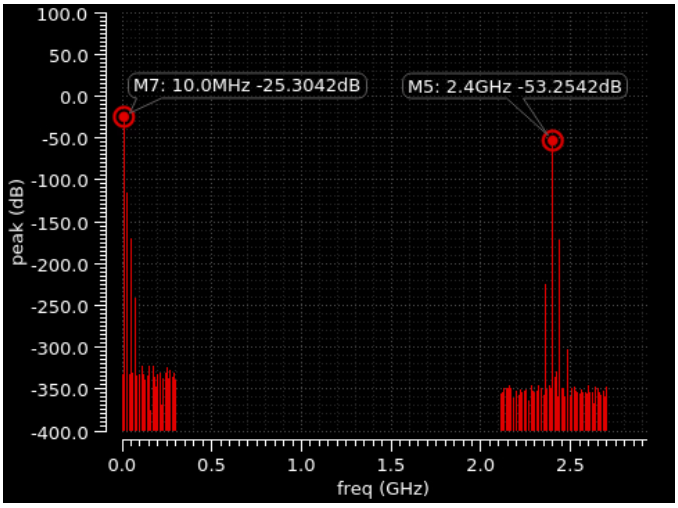

Fig. 13. IF and RF output spectrum with realistic inductor.

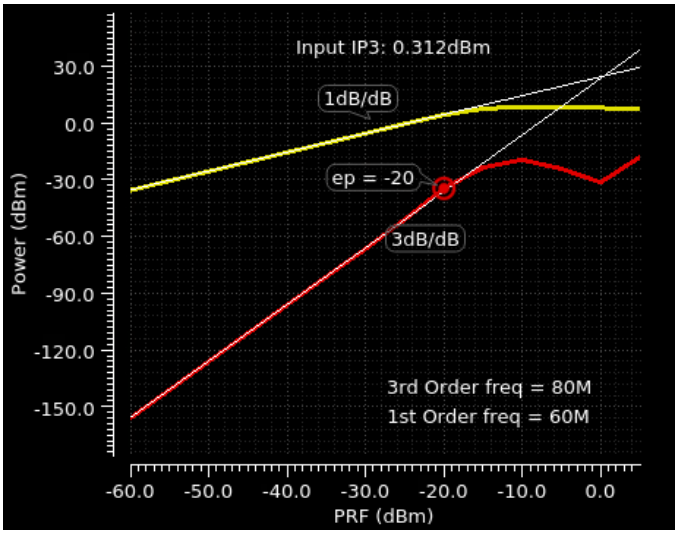

Fig. 14. IIP3 with realistic inductor.

C. System Results and Comparison

The system results are summarized below in Table II. All specifications were gathered for an IF of 10MHz. Comparison to similar direct-conversion receivers with a merged architecture is also given. Overall, the tradeoff between noise figure and IIP3 is challenging, particularly at an extremely lower power as desired.

TABLE II. COMPARISON OF DIRECT-CONVERSION MERGED RECEIVERS

Reference	Frequency [GHz]	Gain [dB]	Noise Figure [dB]	IIP3 [dBm]	Power [mW]
This work	2.4	28	5.33	0.312	9.23
[11]	2.1	23	3.4	-1.5	21.6
[12]	0.1-3.85	12.1	8.4	-12.8	9.8
[13]	1.3-3.3	21.4	4.55	-6.5	16.83
[14]	0.5-7	18	5.5	-3	16

Finally, the transient behavior was verified for the entire frontend with the designed QVCO. The output quadrature IF waveforms for a 7MHz IF are shown below. From these outputs, the signals would be low-pass filtered for channel selection and then passed to the receiver's backend or a variable gain amplifier.

V. CONCLUSION

In this report, the design of a 2.4GHz direct-conversion receiver was discussed, and results were presented. The receiver was fully operational and tested for an IF of approximately 7MHz. The design achieves a conversion gain of 28dB with a noise figure of 5.3dB at IF, and an input-referred IP3 of 0.3dBm. The entire frontend dissipates 9.2mW.

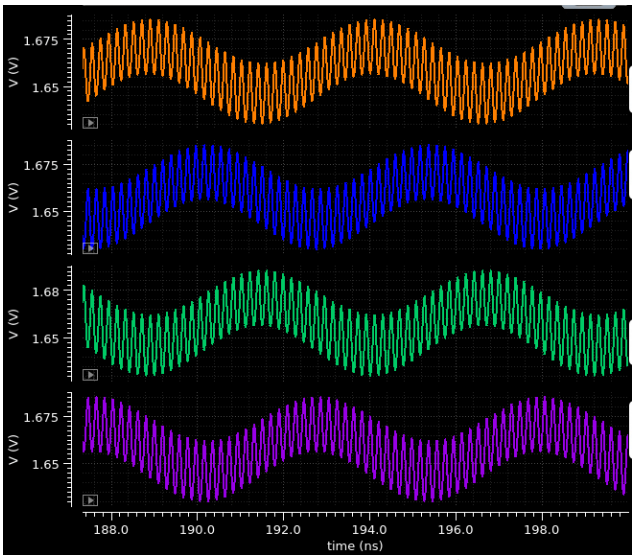

Fig. 15. 7MHZ IF output waveforms

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