VLSI Circuit Design Project Report

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ABSTRACT

In this report, the design and verification of a fully-differential operational amplifier based on a folded cascode topology is discussed. A common-mode feedback circuit is used to set the output common-mode to a desired level based on a provided voltage reference. The circuit achieves a gain-bandwidth product of 122.7 MHz post-layout, with a DC gain of 58.15 dB. Particular attention was given to the noise and linearity performance of the opamp, with an input-referred noise figure of 3.195 nVrms and an IM3 of -62.13 dB post-layout. The total power consumption is 2.268 mW. The tradeoffs, procedures, and layout practices used in the design of the operational amplifier are discussed in this report.

I. Introduction

A fully-differential operational amplifier (op-amp) is a type of electronic device that is used to amplify the difference between two input signals. Unlike traditional op-amps, fully differential op-amps contain a differential output, allowing them to accurately measure and amplify very small differences between the two input signals. This makes them particularly useful in applications where precision and accuracy are critical, such as in instrumentation and medical equipment. Additionally, because they are fully differential, these op-amps are more immune to common-mode noise, making them more resistant to interference and highly reliable in noisy environments.

Several topologies exist for the implementation of this kind of device, including both one and two stage designs. In a one-stage design, the small-signal current flows directly through the output, and thus the gain of such a design is limited directly by the output impedance. For applications in which the output or load impedance is very small, the use of a two-stage topology is required to buffer the gain stage from the output impedance loading. Another useful characteristic of two-stage topologies is the possibility to incorporate a gain stage followed by a stage providing large output swing. In modern CMOS processes where the supply voltage is often limited to 1.8V or less, this type of design is highly useful for applications where a large output swing is needed. To determine the best design for the applications relevant to this project, the tradeoffs of various designs must be considered. A summary of design tradeoffs for various topologies is shown below in Table I [1].

TABLE I
COMPARISON OF PERFORMANCE OF VARIOUS OP-AMP TOPOLOGIES

Topology	Gain	Output Swing	Speed	Power Dissipation	Noise	Complexity
Telescopic	Low	Medium	Highest	Low	Low	Low
Folded Cascode	Medium	Medium	High	Medium	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low	High
Gain-Boosted	High	Medium	Medium	High	Medium	High

In the end, the folded cascode topology was chosen for its all-around good performance and manageable complexity. This design also allows for the ability to choose the same input and output common-mode level, an extremely useful design tool for when working with common-mode feedback. The folded cascode amplifier also allows for larger output swings than other one-stage designs.

II. Design and Calculations

For both circuits in the op-amp design, hand calculations were done according to the specifications to determine rough device aspect ratios and were used as a starting point when simulating the circuit. In simulation, the design was modified to meet the desired specifications.

A. Folded Cascode Op-Amp Circuit

The schematic of the folded cascode op-amp is shown below in Fig. 1 [1].

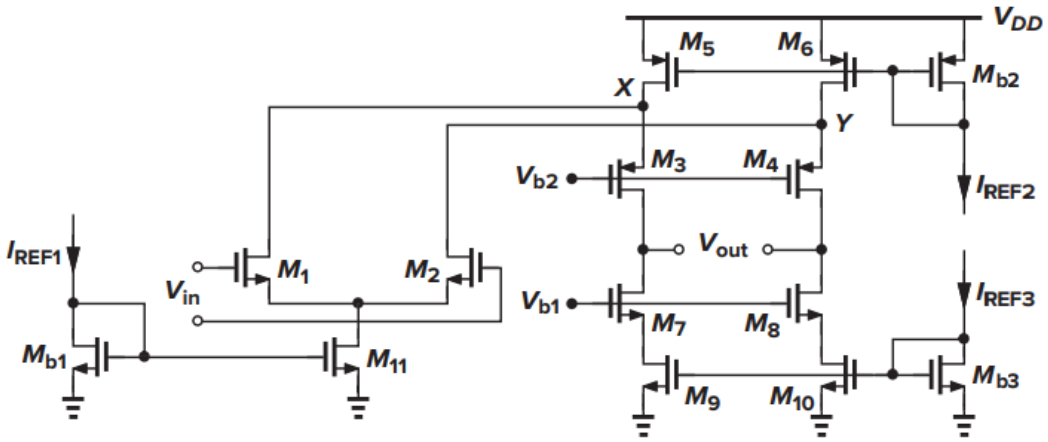

Figure 1: Folded Cascode Op-Amp Schematic

To begin, the power budget (3 mW) is considered, and branch currents are assigned relative to this value and the desired gain. For this design, the drain current through M1 and M2 was set to be 150µA to provide a large gain through the first common-source stage. The drain current through M5 and M6 was set to be 450µA to provide adequate output swing and to meet the slew rate specification. Given that the load capacitance is 2.5pF, the slew rate can be found as (1)

$$SR = \frac{I_{D4}}{C_L} \tag{1}$$

To meet the specification of 75 V/µs, a drain current of 300µA is needed, thus 450µA through M5 and M6 as chosen above.

Next, overdrive voltages for each pair of devices were chosen to allow for sufficient gain and transconductance while having enough headroom for the drain-source voltages of each device. Further assuming an output common-mode level of 900mV, we can allocate 900mV to M3/4 and M5/6 and 900mV to M7/8 and M9/10. Since M5 and M6 are carrying the most current, we will allocate 500mV of overdrive voltage to it, leaving 400mV for M3/4. On the bottom of the cascode structure, we allocate 300mV to M7/8 and M9/10 to leave some headroom for any variations. Using the overdrive voltages and drain currents for each pair of devices, the aspect ratios can be found from (2)

$$\left(\frac{W}{L}\right) = \frac{2I_D}{\mu C_{ox} V_{ov}^2} \tag{2}$$

Working with the input common-mode voltage of 900mV and allocating an overdrive voltage of 400mV for M11, the overdrive voltage of M1/2 can be calculated and used with the drain current to calculate aspect ratio. A similar procedure is used to find the aspect ratio of M11. For MB1, MB2, and MB3, a 1:1 mirroring ratio is assumed. For all devices, a length of 360nm was used to provide adequate gain and limit the effects of channel-length modulation. The calculated device sizes and aspect ratios are summarized below in Table II.

TABLE II
FOLDED CASCODE CALCULATED DEVICE PARAMETERS

Device	Aspect Ratio	Width	Length
M1/M2	150	54 µm	360 nm
M3/M4	37.5	14 µm	360 nm
M5/M6/MB2	72	26 µm	360 nm
M7/M8	33.33	12 µm	360 nm
M9/M10/MB3	33.33	12 µm	360 nm
M11/MB1	18.75	7 µm	360 nm

To allow for sufficient losses in the current mirrors due to lambda effects, I_{REF1} was chosen as 400µA and I_{REF2} was chosen as 250µA. I_{REF3} is implemented by the common-mode feedback circuit which will be discussed in the next section. All bias and common-mode voltages were designed to be 900mV to utilize the input voltage reference provided to the chip.

B. Common-Mode Feedback Circuit

The principle of common-mode feedback is to utilize negative feedback to set the common-mode voltage output to a desired level. To utilize this principle with the folded cascode amplifier, the negative feedback was realized through current feedback to set the base voltage of M9/10 and thus adjust the common-mode output level. A CMFB circuit similar to the design used in [2] has been adapted for use with the folded cascode amplifier. The schematic of the circuit is shown below in Fig. 2.

The circuit is a simple comparator structure, where the output DC level is compared to a provided reference. Current passed through the differential pairs is generated in the top PMOS devices, which is then passed through as negative feedback to the folded cascode circuit. All PMOS devices were designed with an aspect ratio of approximately 11, to provide adequate loop gain and amplification of differences. The NMOS current mirror and dummy load devices were matched to the size of M9/M10 in the folded cascode circuit. A length of 180nm was used for all devices. A summary of the device parameters used is listed below in Table III.

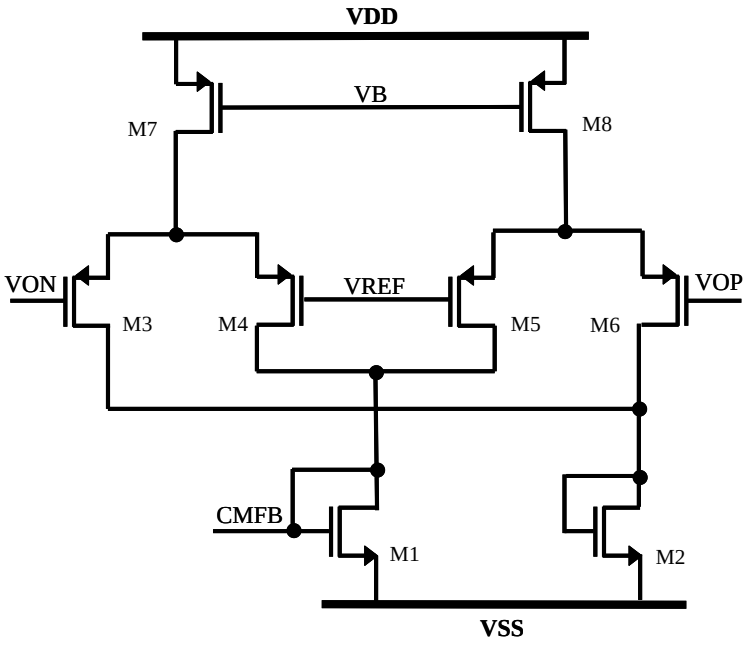

Figure 2: CMFB Circuit

TABLE III
CMFB CALCULATED DEVICE PARAMETERS

Device	Width	Length
M1/M2	12 µm	180 nm
M3/M4	2 µm	180 nm
M5/M6	2 µm	180 nm
M7/M8	2 µm	180 nm

D. Simulation Adjustments

After obtaining a starting point for the device sizes, the circuits were simulated and adjusted accordingly to meet the desired specifications. The final schematic of the folded cascode is shown below in Fig. 3. One significant change that was made was the addition of devices to assist during slewing. The NMOS devices MC1 and MC2 assist with the slew rate by clamping V_{D1} and V_{D2} during slewing. The result is a much higher slew rate. Some other modifications were made to device sizes and bias currents based on parameters such as gain or power consumption. The final values of devices in the folded cascode circuit are summarized in Table IV.

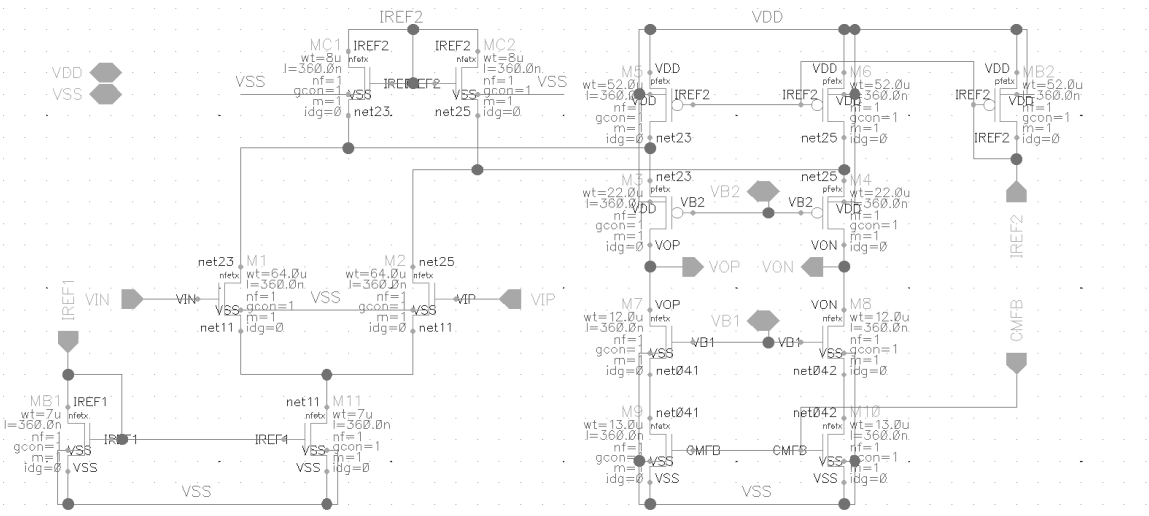

Figure 3: Folded Cascode Simulation Schematic

TABLE IV
FOLDED CASCODE FINAL DEVICE PARAMETERS

Device	Width	Length
M1/M2	64 µm	360 nm
M3/M4	22 µm	360 nm
M5/M6/MB2	52 µm	360 nm
M7/M8	12 µm	360 nm
M9/M10/MB3	13 µm	360 nm
M11/MB1	7 µm	360 nm
MC1/MC2	8 µm	360 nm

The CMFB circuit was also simulated with calculated parameters, with no changes being made to the device sizes. The schematic is shown below in Fig. 4.

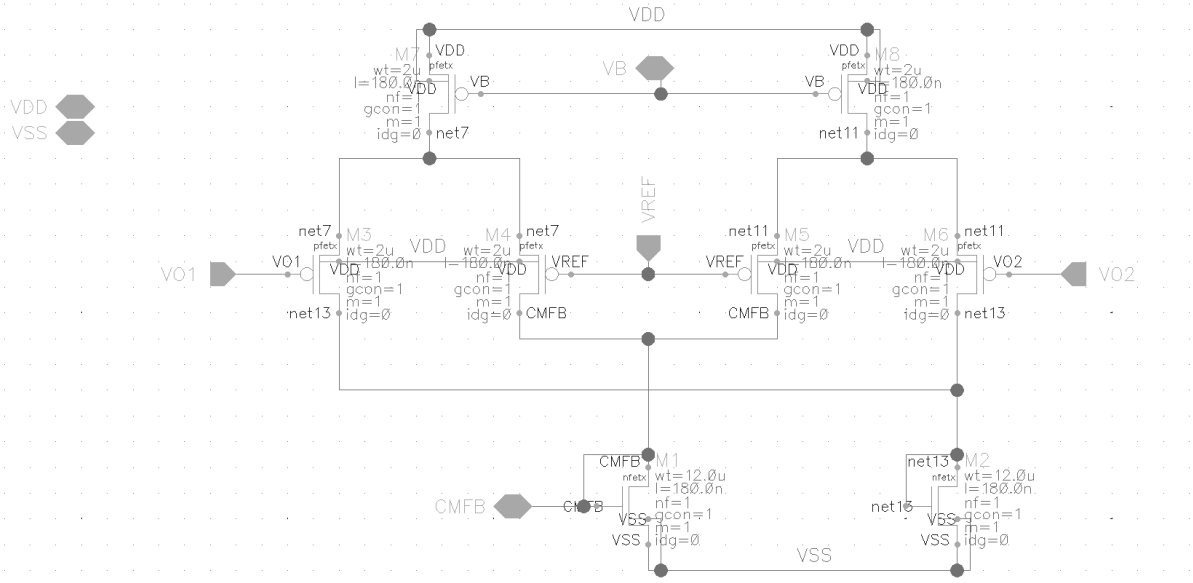

Figure 4: CMFB Simulation Schematic

In order to provide the necessary bias currents to the folded cascode circuit, a small block consisting of current mirrors providing the necessary currents and correct polarities was implemented using the 100µA bias current provided to the device. The schematic and device sizes are shown below in Fig. 5.

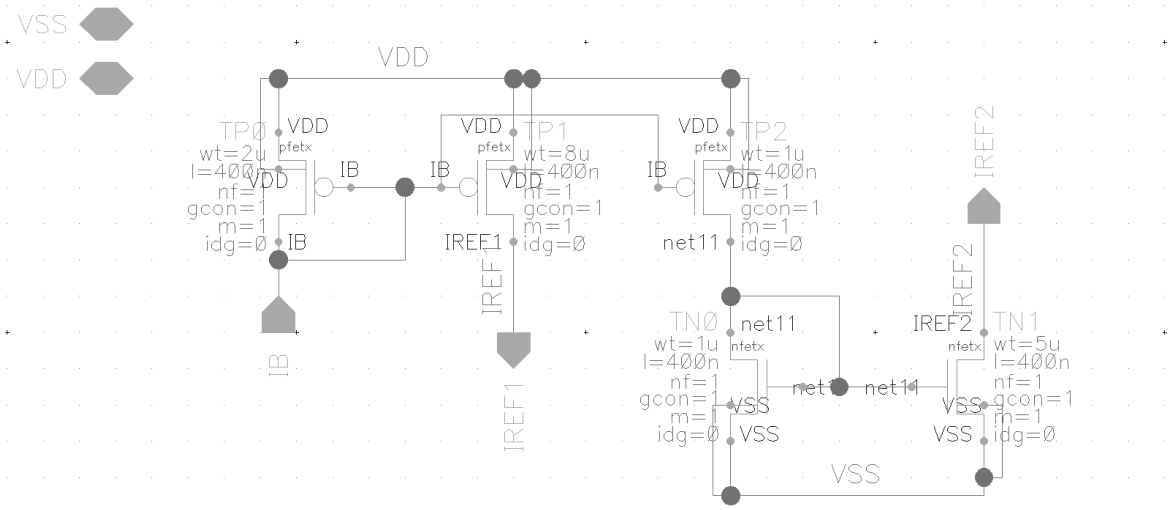

Figure 5: Current Bias Schematic

Finally, with all the sub-blocks created, a top-level cell view of the op-amp was created to interconnect the various blocks and provide the correct names for input and output pins. The top-level view is shown in Fig. 6.

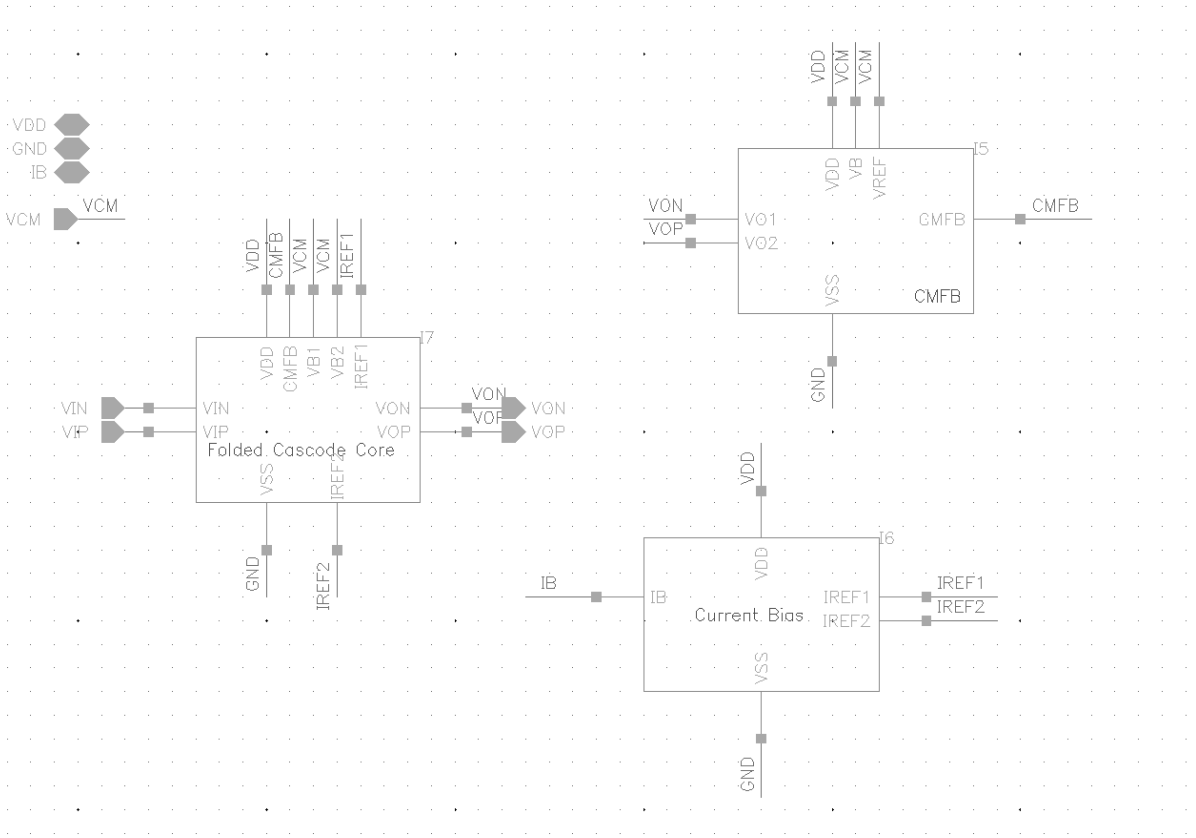

Figure 6: Op-Amp Top Level Schematic

In order to correctly verify the circuit, two primary test benches were used in conjunction with an ADE XL state to compile and calculate the results. Both an open-loop case (Fig. 7) and closed-loop case (Fig. 8) were used.

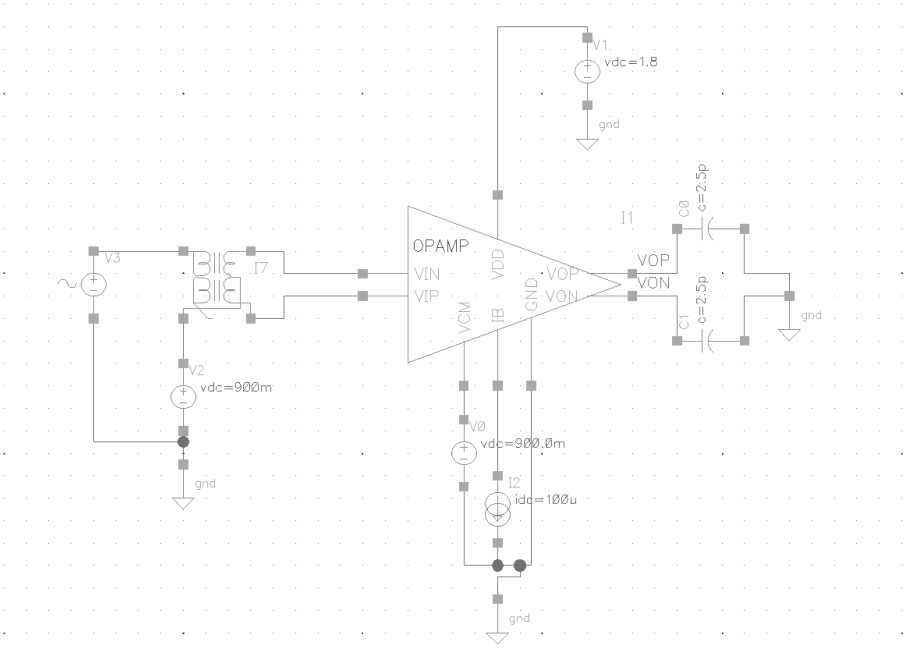

Figure 7: Open Loop Test Bench

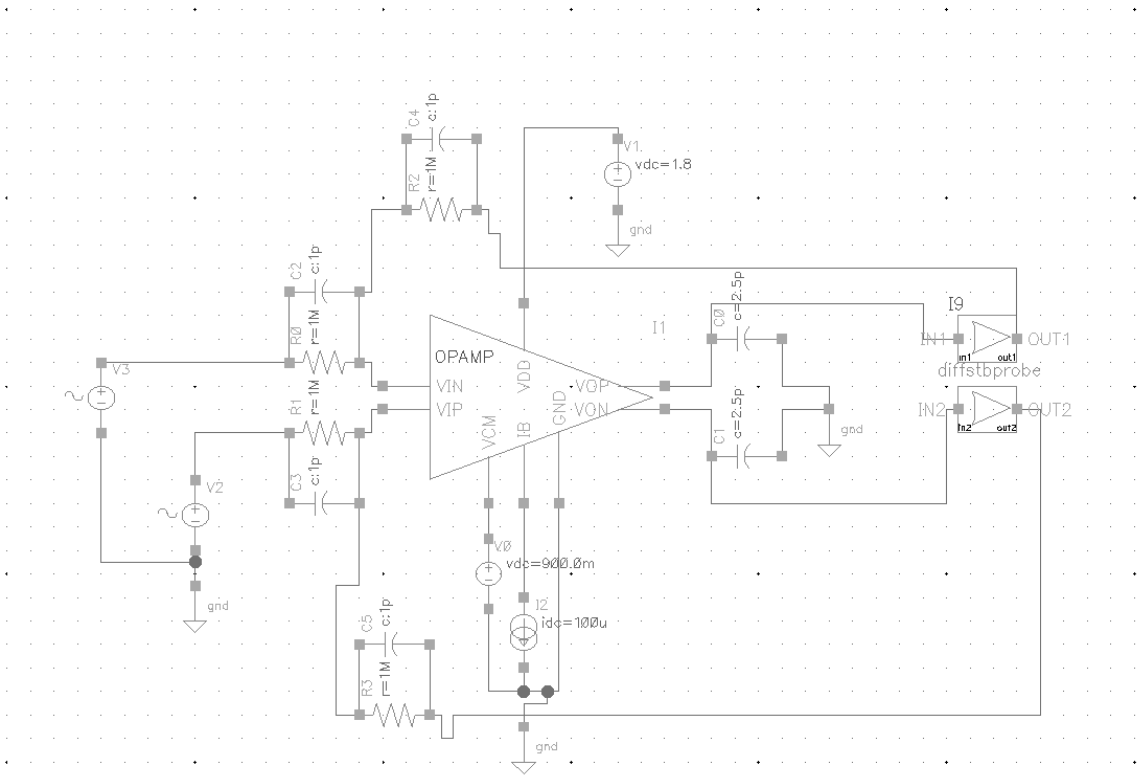

Figure 8: Closed Loop Test Bench

III. PRE-LAYOUT RESULTS

The pre-layout simulation results for key parameters are summarized below in Table V. The ADE XL results are also shown in Fig. 9.

TABLE V
PRE-LAYOUT SIMULATION RESULTS

Parameter	Specification	Simulation Result
Power Dissipation	≤ 3mW	2.533mW
DC Gain	≥ 60 dB	61.52 dB
GBW	≥ 120 MHz	158 MHz
Slew Rate	≥ 75 V/µs	75.59 V/µs
Input-Referred Noise	≤ 50 µVrms	3.967 nVrms
IM3	≤ -60 dB	-61.77 dB
Differential Phase Margin	≥ 60°	82.54°
CMFB Phase Margin	≥ 60°	111.1°

Test	Output	Nominal	Spec	Weight	Pass/Fail
opamp_ol_dc	ISUPPLY				
opamp_ol_dc	POWER	2.533 mW	< 3m		pass
opamp_ol_dc	/VOP				
opamp_ol_dc	/VON				
opamp_ol_dc	VCM-	898.6 mV	range 875m 925...		pass
opamp_ol_dc	VCM+	898.6 mV	range 875m 925...		pass
opamp_ol_ac	/VOP				
opamp_ol_ac	/VON				
opamp_ol_ac	Open Loop Gain				
opamp_ol_ac	AV0	61.52 dB	> 60		pass
opamp_ol_ac	GBW	158 MHz	> 120M		pass
opamp_ol_noise	Input Noise				
opamp_ol_noise	Input Noise Integ	3.967 nVrms	< 50u		pass
opamp_ol_slew	/VOP				
opamp_ol_slew	/VON				
opamp_ol_slew	SR	75.59 MV/us	> 75M		pass
opamp_cl_pm	Phase Margin	82.54 deg	> 60		pass
opamp_cl_pm	Loop Gain Phase				
opamp_cl_pm	Loop Gain dB20				
opamp_cl_im3	Spectrum				
opamp_cl_im3	IM3	61.77 dB	> 60		pass
opamp_cl_cmfb	CM Loop Gain P...				
opamp_cl_cmfb	CM Loop Gain d...				
opamp_cl_cmfb	CM Phase Margin	111.1 deg	> 60		pass

Figure 9: ADE XL Pre-Layout Summary

The plot for the AC simulation of DC gain and gain-bandwidth product are shown in Fig. 10. The open-loop test bench was used for this specification.

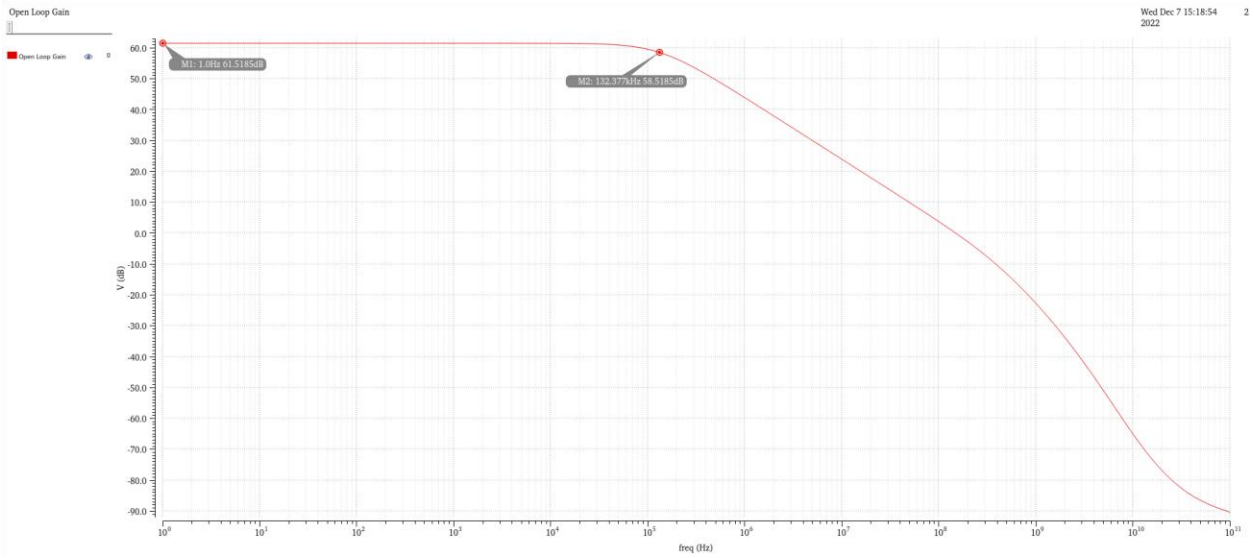

Figure 10: Pre-Layout AC Simulation

The plot for the input-referred noise is shown in Fig. 11. The open-loop test bench was used for this specification.

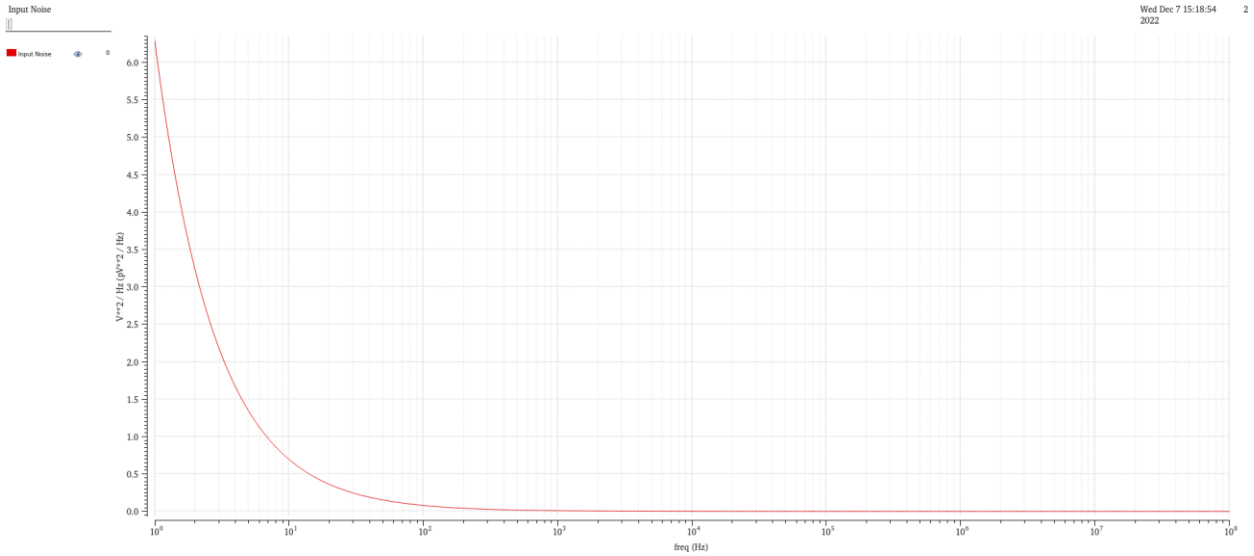

Figure 11: Pre-Layout Input-Referred Noise Simulation

The plot for the transient simulation of slew rate is shown in Fig. 12. The open-loop test bench was used for this specification.

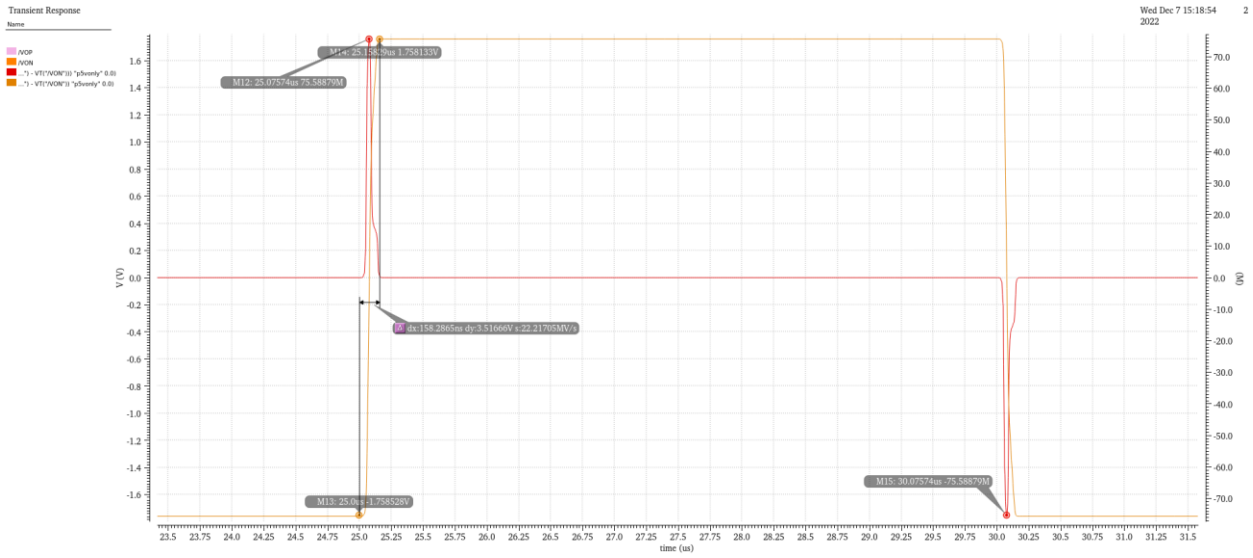

Figure 12: Pre-Layout Transient Simulation

The plot for the spectrum and IM3 measurement is shown in Fig. 13. The closed-loop test bench was used for this specification.

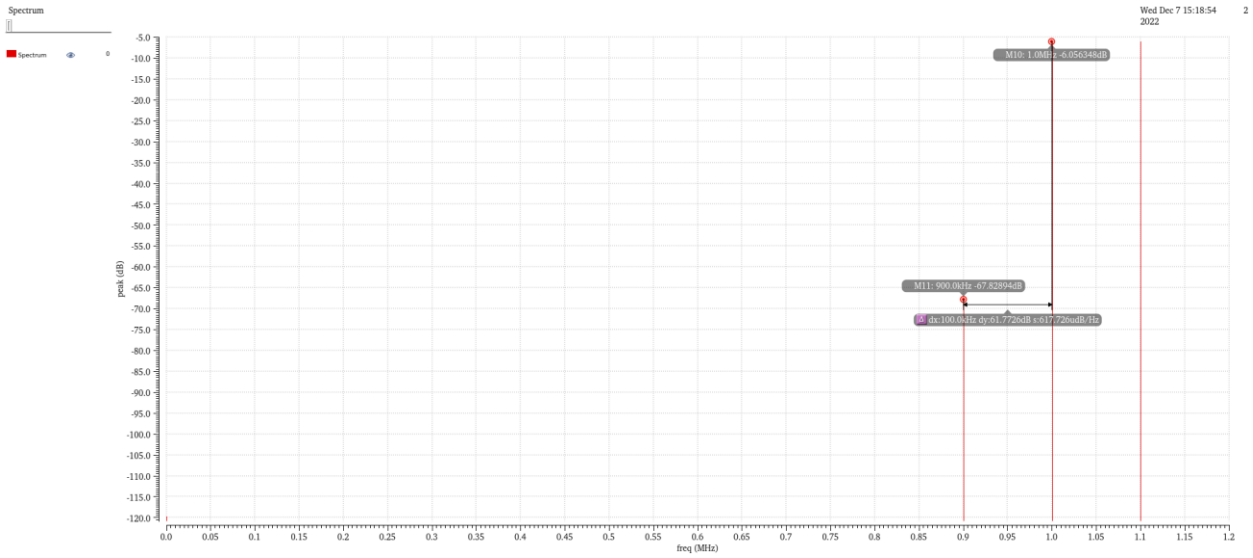

Figure 13: Pre-Layout IM3 Simulation

The plot for the differential phase margin is shown in Fig. 14. The closed-loop test bench was used for this specification.

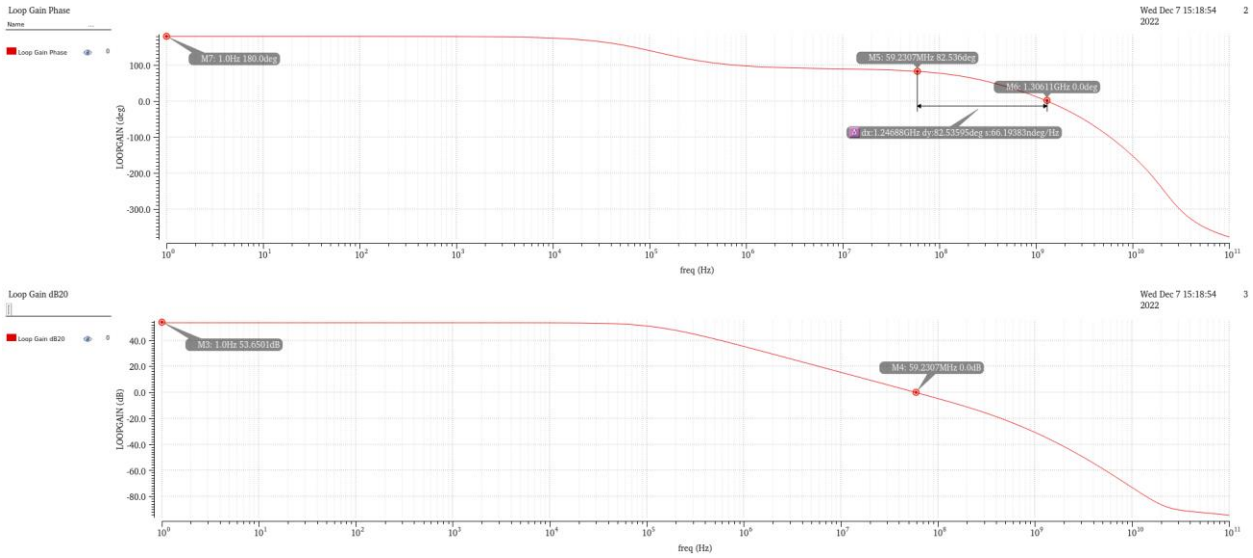

Figure 14: Pre-Layout Differential Phase Margin Simulation

Finally, the plot for the common mode feedback phase margin is shown in Fig. 15. The closed-loop test bench was used for this specification.

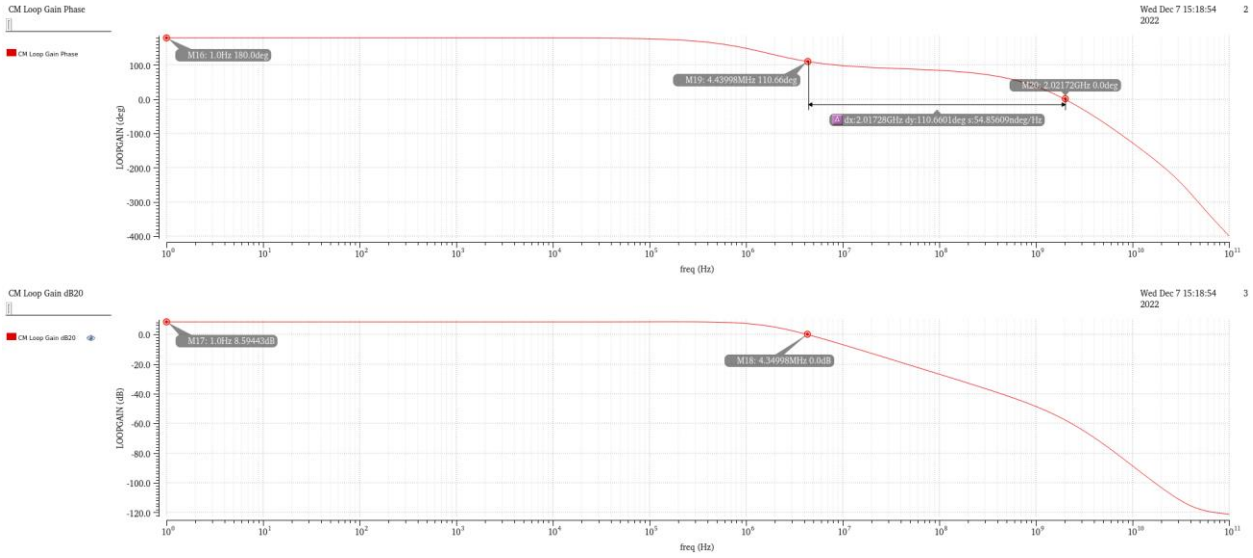

Figure 15: Pre-Layout CMFB Phase Margin Simulation

IV. LAYOUT

To begin, the layout of the folded cascode was completed. Finger widths of 1µm were used. Good layout practices such as matching, dummy elements, and guard rings were used in the layout. An additional guard ring was placed around the PMOS devices to reduce the likelihood of latch-up and ensure a low-impedance path to ground exists in the substrate. The finalized layout of this block is shown in Fig. 16. The layout was also successfully verified using DRC and LVS (Fig. 17).

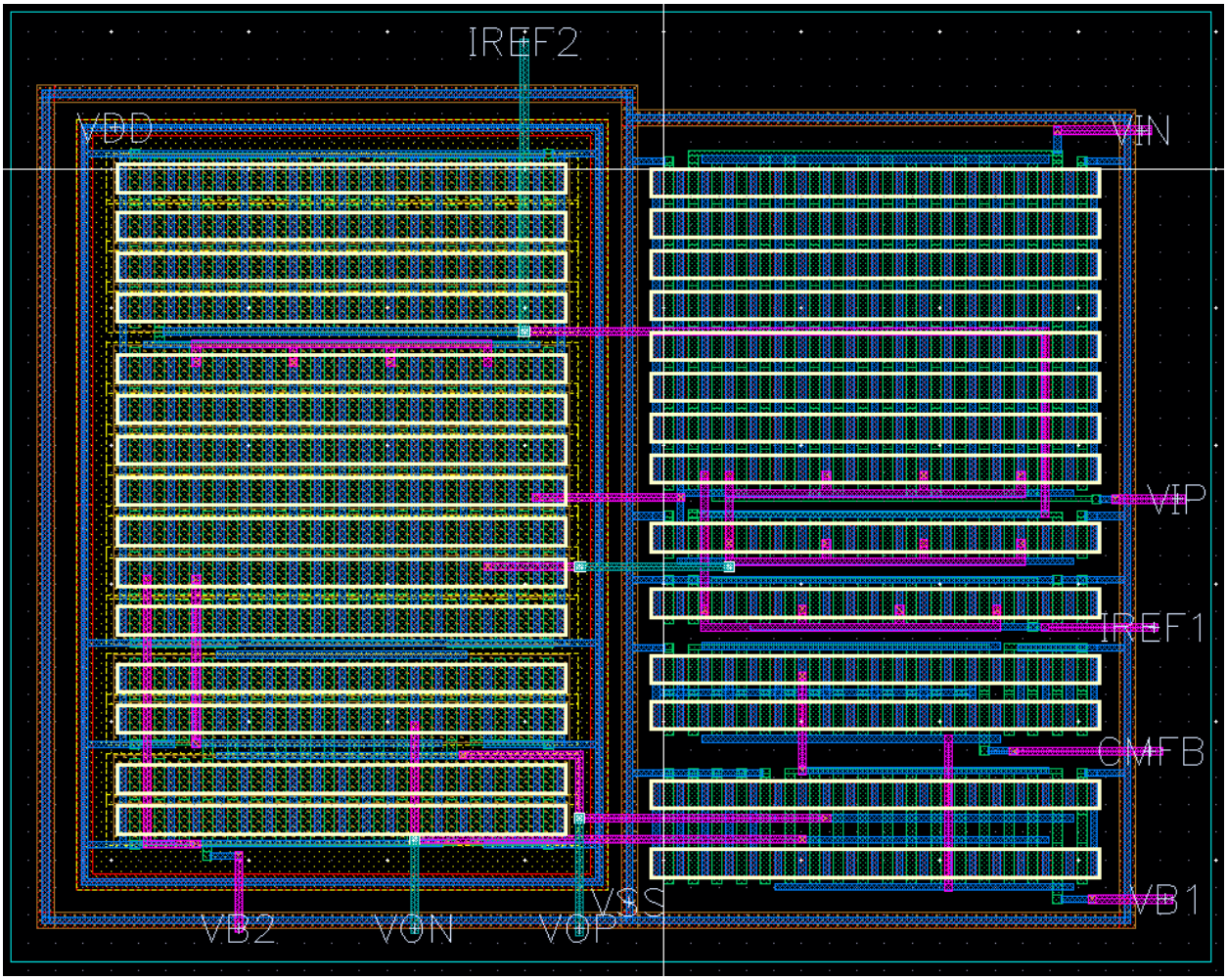

Figure 16: Folded Cascode Layout

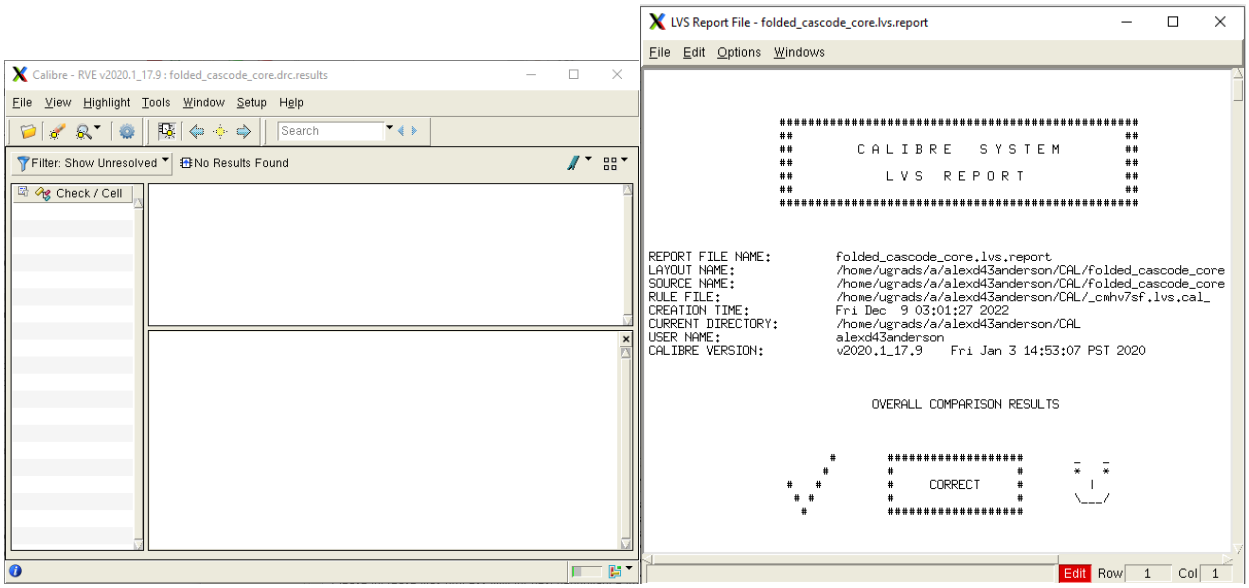

Figure 17: Folded Cascode DRC and LVS

Next, the layout for the common-mode feedback block was performed (Fig. 18). Similar layout practices were used, and the design was verified using DRC and LVS (Fig. 19).

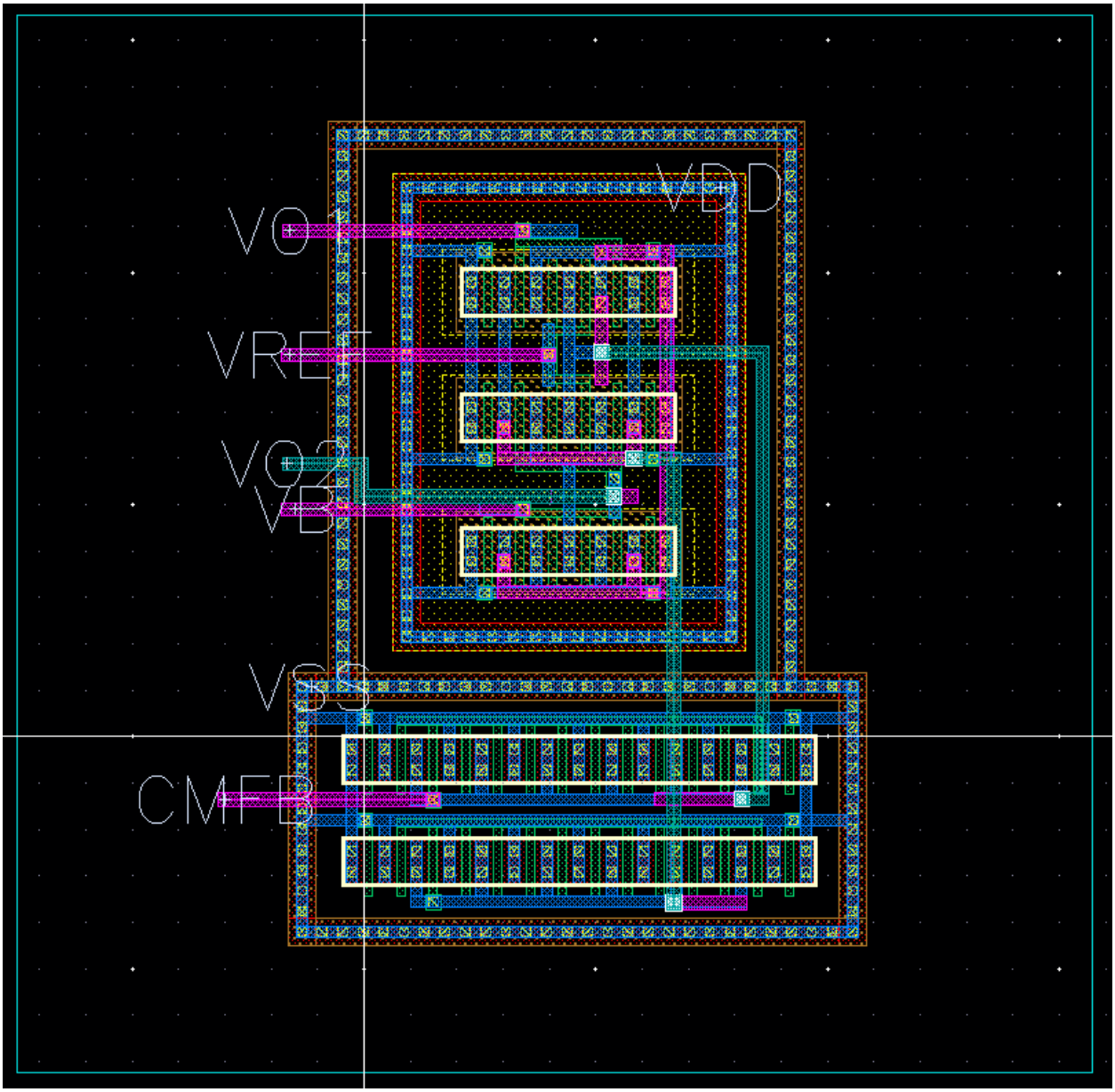

Figure 18: CMFB Layout

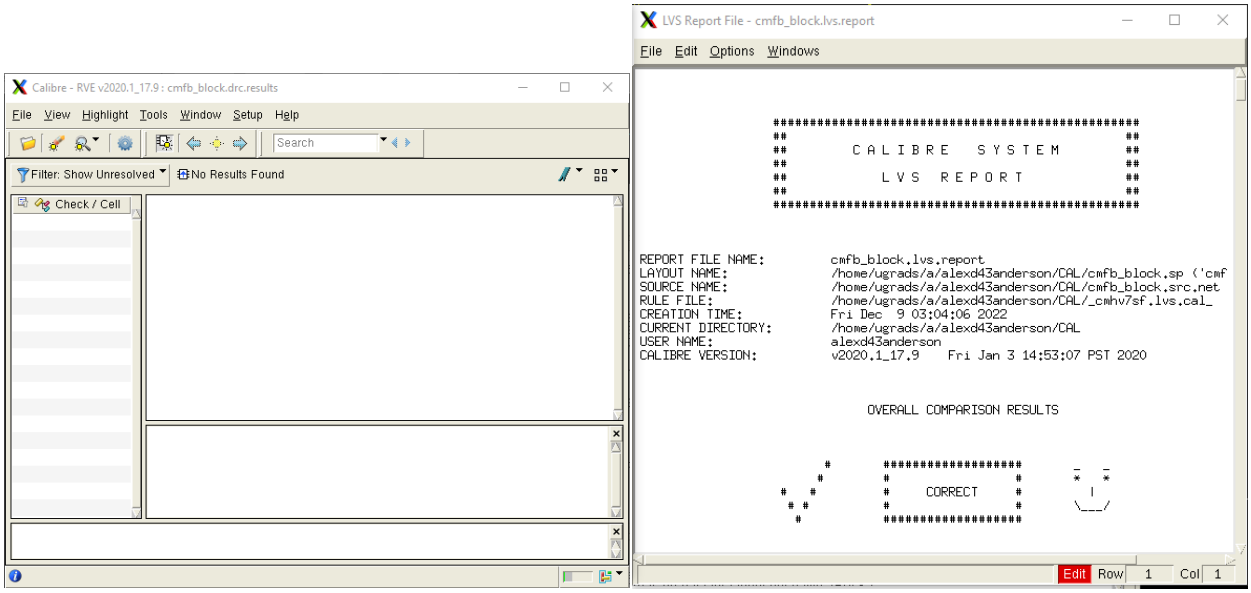

Figure 19: CMFB DRC and LVS

Next, the layout for the current bias block was performed (Fig. 20). Similar layout practices were used, and the design was verified using DRC and LVS (Fig. 21).

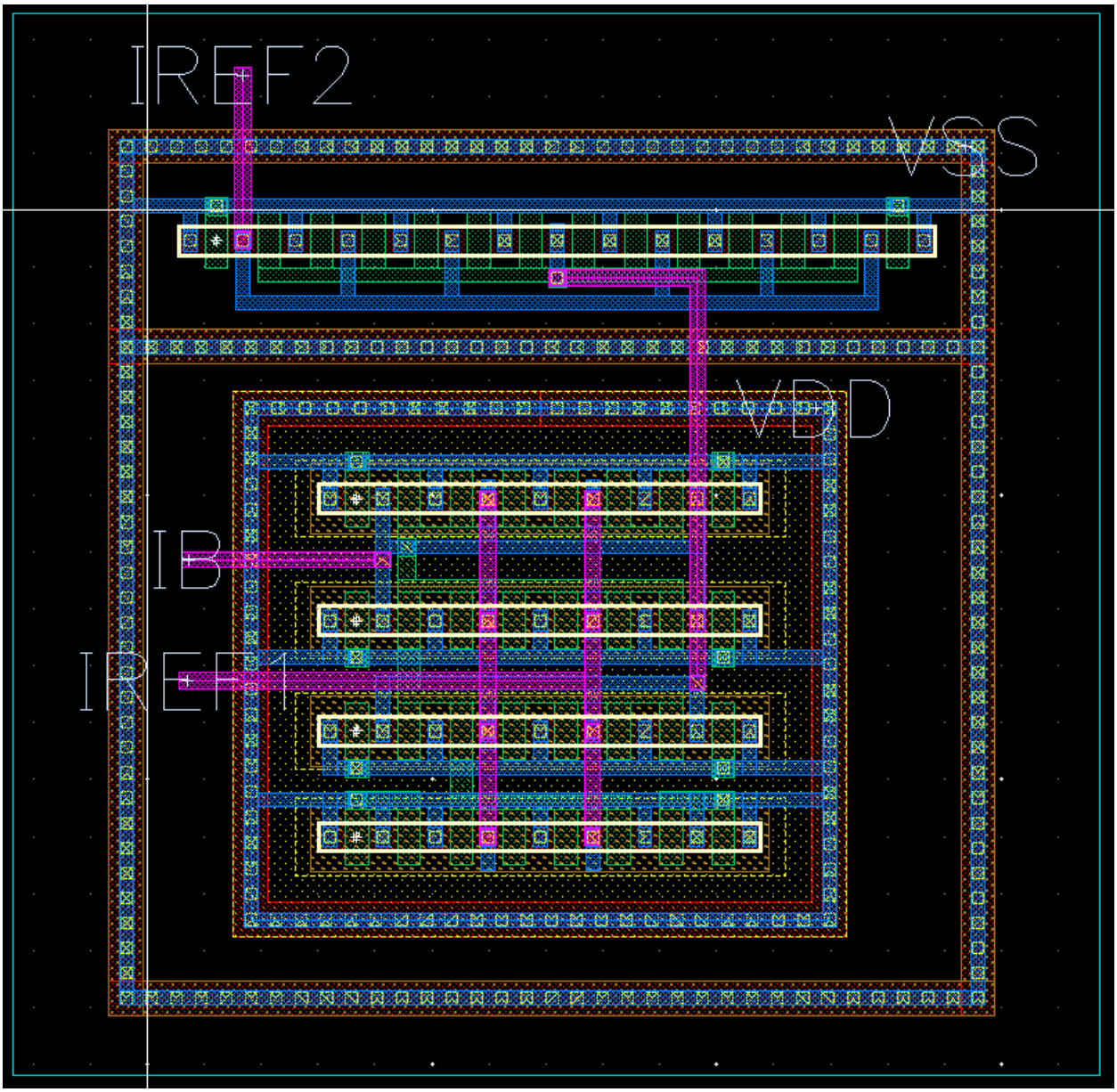

Figure 20: Current Bias Layout

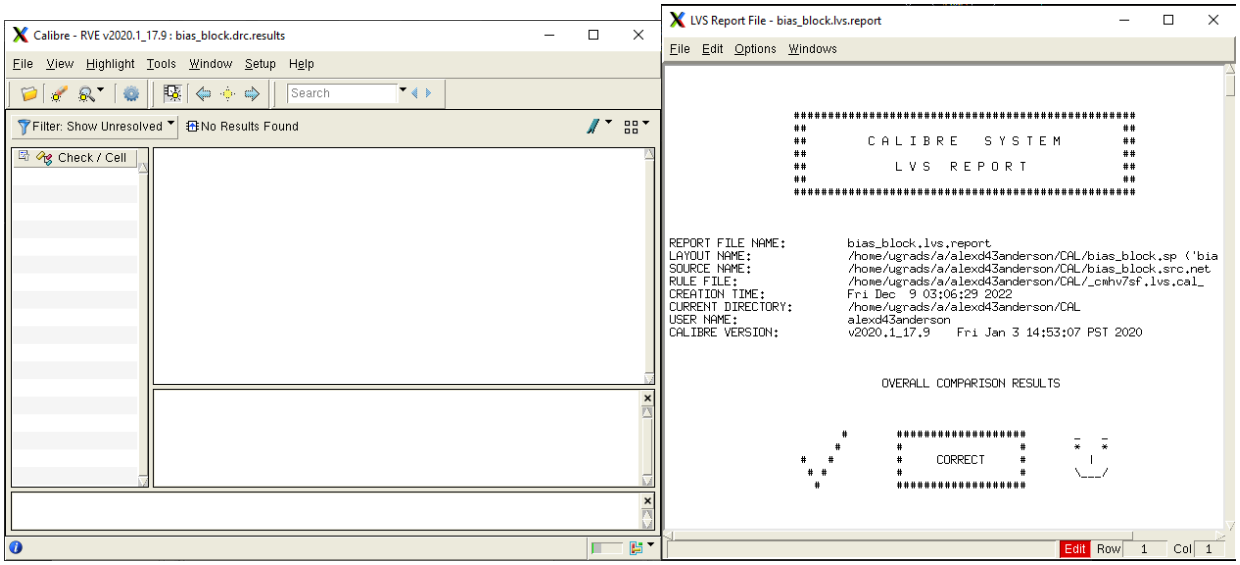

Figure 21: Current Bias DRC and LVS

Finally, the top level of the chip was created by placing down each of the previously shown layouts and interconnecting them accordingly (Fig. 22). The final pins were placed on metal 4. The top level layout was also verified using DRC and LVS (Fig. 23).

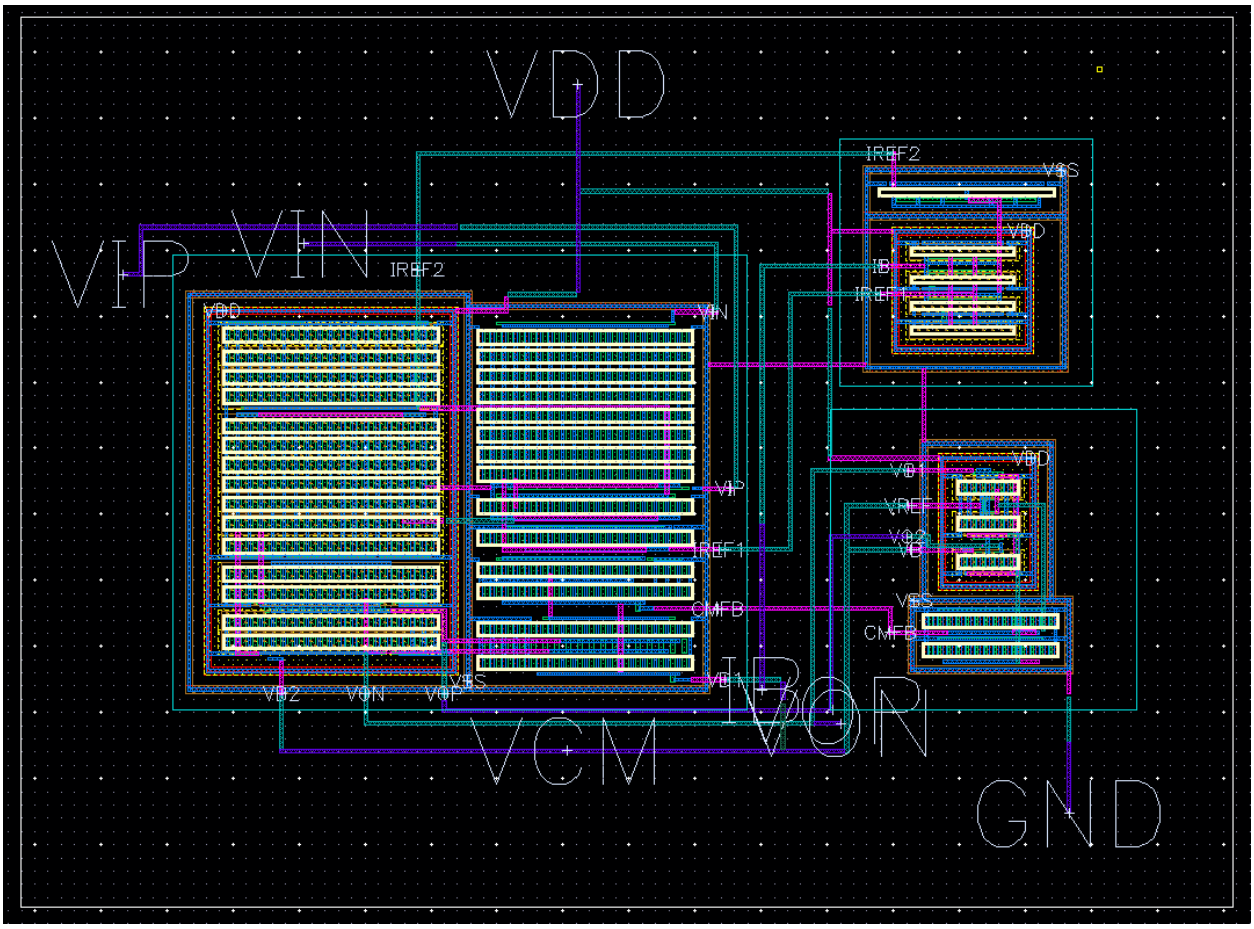

Figure 22: Top Level Layout

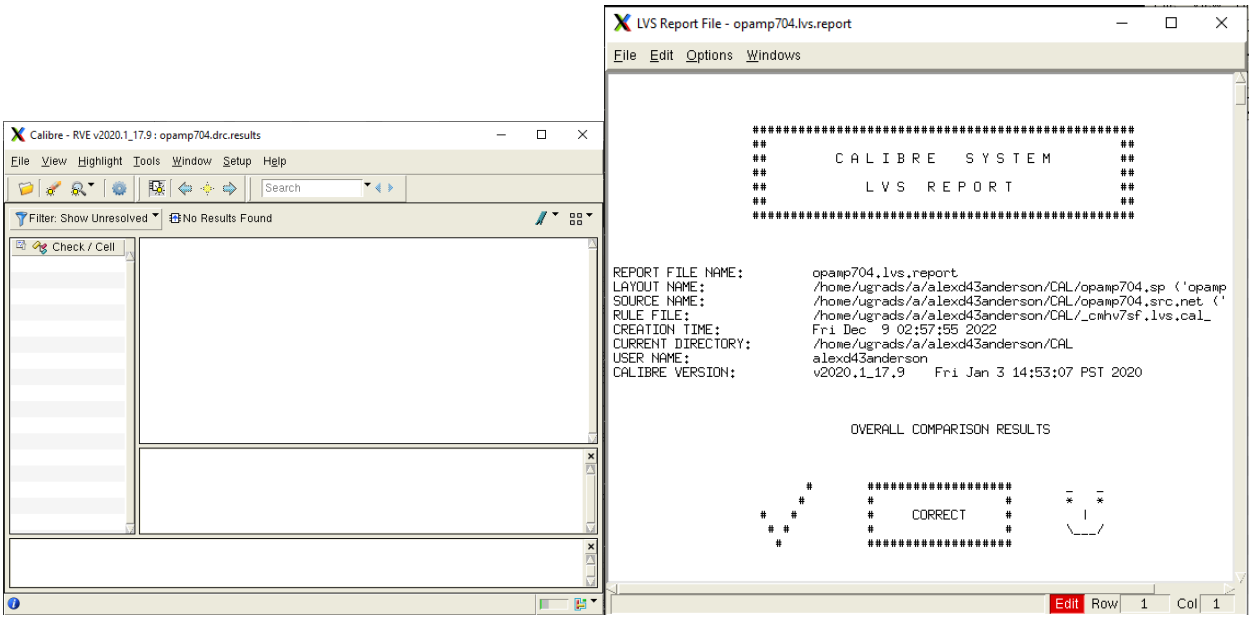

Figure 23: Top Level DRC and LVS

From here, the parasitics were extracted from each level of the hierarchy and used to perform post-layout simulations.

V. Post-Layout Results

The post-layout simulation results for key parameters are summarized below in Table VI.

TABLE VI
POST-LAYOUT SIMULATION RESULTS

Parameter	Specification	Simulation Result
Power Dissipation	≤ 3mW	2.268mW
DC Gain	≥ 60 dB	58.15 dB
GBW	≥ 120 MHz	122.7 MHz
Slew Rate	≥ 75 V/µs	58.87 V/µs
Input-Referred Noise	≤ 50 µVrms	3.195 nVrms
IM3	≤ -60 dB	-62.13 dB
Differential Phase Margin	≥ 60°	84.99°
CMFB Phase Margin	≥ 60°	107.8°

The plot for the AC simulation of DC gain and gain-bandwidth product are shown in Fig. 24. The DC gain decreased about 3dB, likely due to losses associated with parasitic resistances of traces, vias, and devices. The bandwidth increased slightly, likely due to parasitic capacitance adding a zero to the transfer function. For these reasons, the gain-bandwidth product fell but remained above the 120 MHz specification.

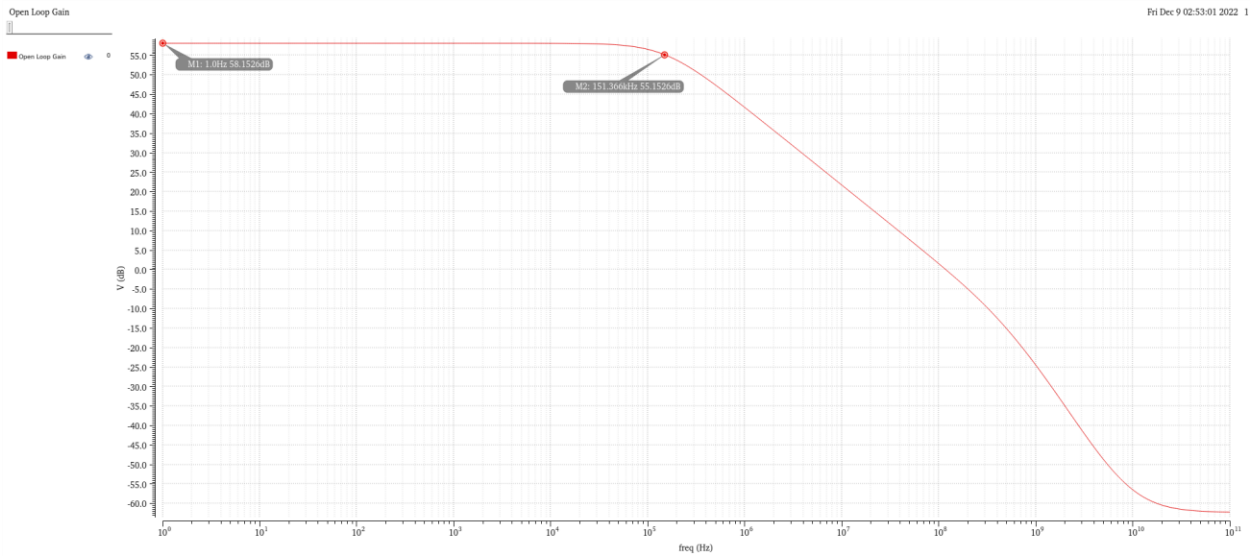

Figure 24: Post-Layout AC Simulation

The plot for the input-referred noise is shown in Fig. 25. The noise values remained relatively the same, even decreasing slightly post-layout.

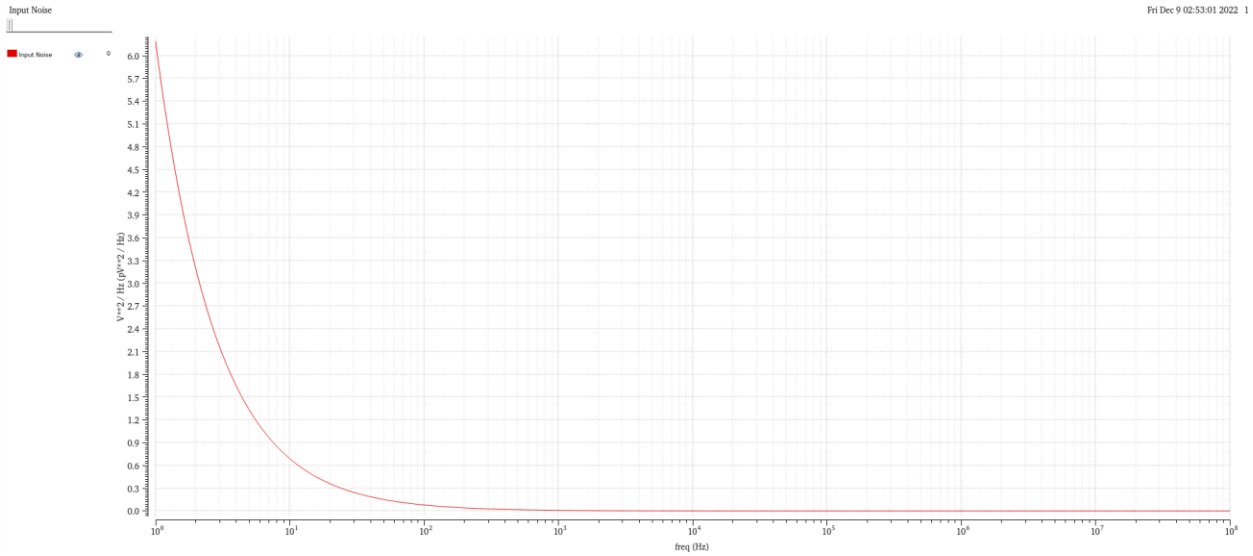

Figure 25: Post-Layout Input-Referred Noise Simulation

The plot for the transient simulation of slew rate is shown in Fig. 26. The slew rate fell drastically post-layout due to the added output capacitance from long traces needed for the output pins. The slew rate is highly sensitive to the load capacitance, causing it to decrease quickly with even a slight increase in this value. Changes in DC current values and bias points also played a role in the decrease of this parameter.

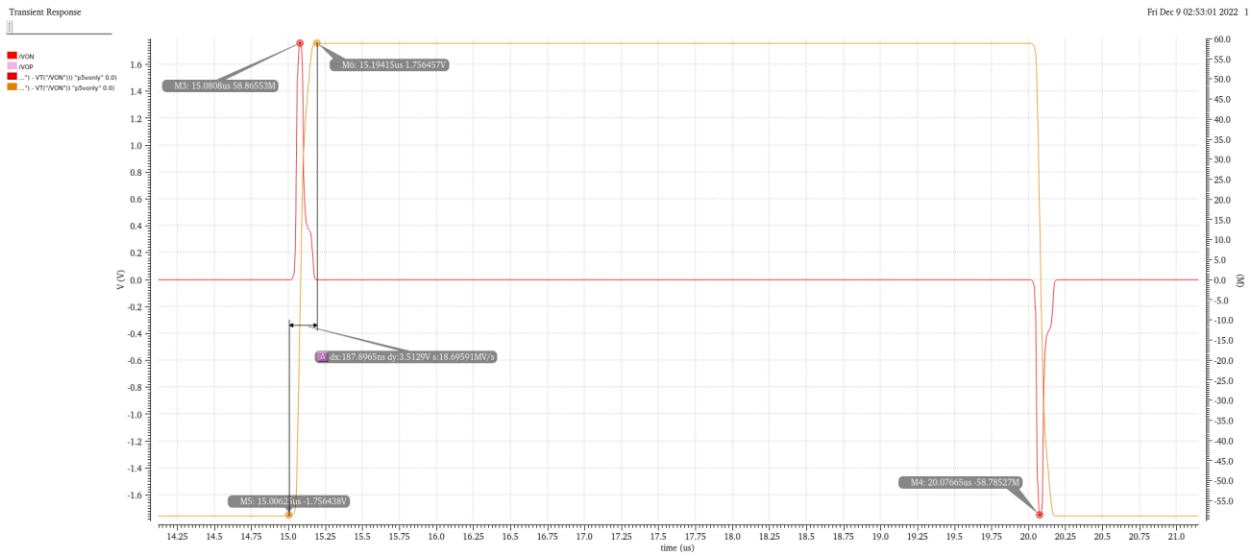

Figure 26: Post-Layout Transient Simulation

The plot for the spectrum and IM3 measurement is shown in Fig. 27. The IM3 value remained relatively the same, even increasing slightly post-layout, similar to the input-referred noise.

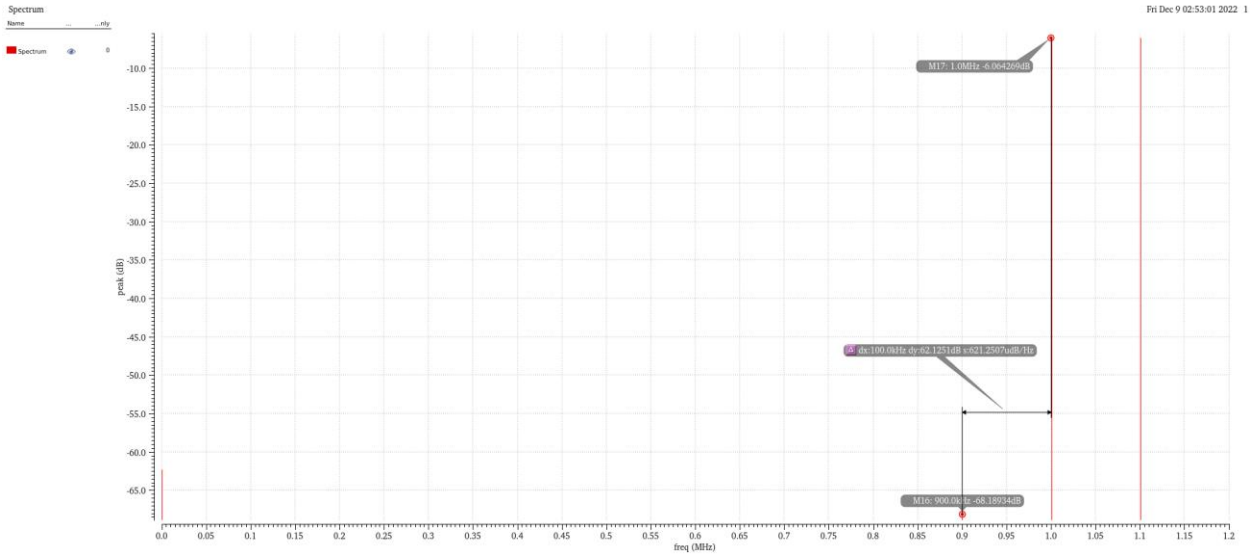

Figure 27: Post-Layout IM3 Simulation

The plot for the differential phase margin is shown in Fig. 28. The phase margin increased slightly post layout due to the increase in output capacitance and perhaps increased transconductance of M3 and M4. This change is also reflected in the reduction of DC gain.

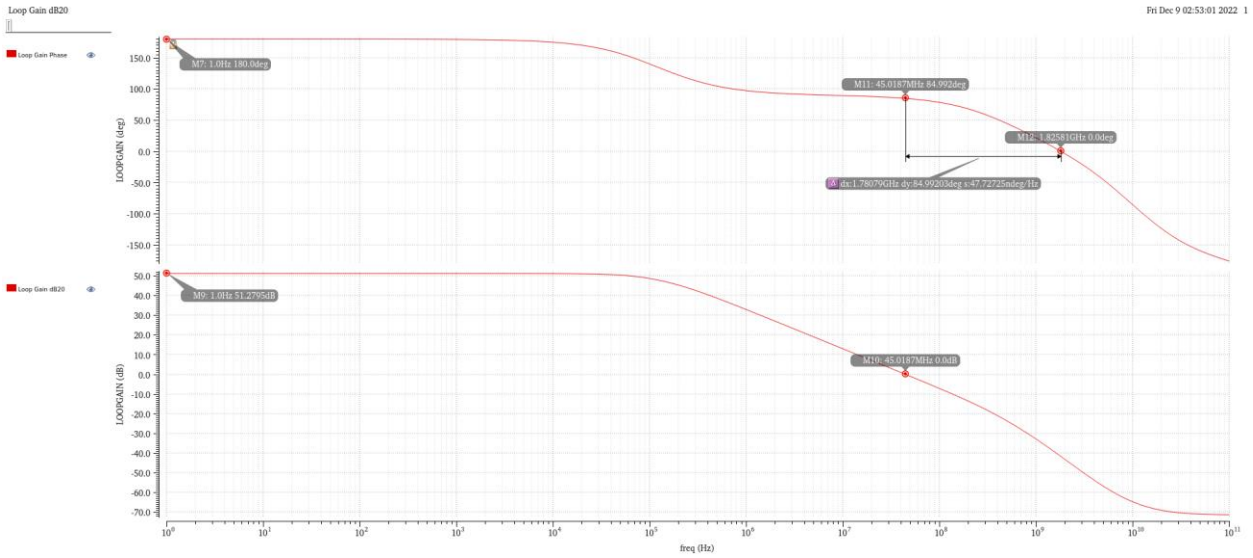

Figure 28: Post-Layout Differential Phase Margin Simulation

Finally, the plot for the common mode feedback phase margin is shown in Fig. 29. The CMFB phase margin decreased slightly post-layout due to the block's increased loop gain.

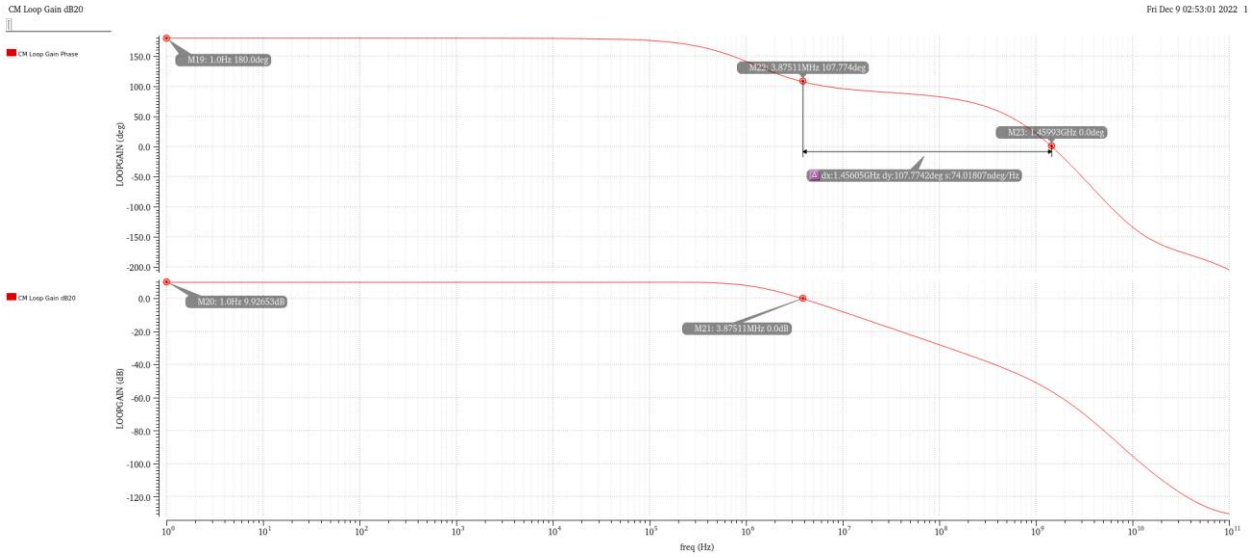

Figure 29: Post-Layout CMFB Phase Margin Simulation

VI. CONCLUSION

In this project, a fully-differential operational amplifier with common-mode feedback was designed. A folded cascode topology was used in order to achieve sufficient gain, speed, and output swing. The folded cascode amplifier, common-mode feedback circuit, and current bias block were designed, simulated, and laid out on a full-scale chip level. Post layout, the circuit achieves a DC gain of 58.15 dB, a gain-bandwidth product of 122.7 MHz, an input-referred noise performance of 3.195 nV_{rms}, an IM3 of -62.13 dB, a slew rate of 58.87 V/μs, a power consumption of 2.268 mW, a differential phase margin of 84.99 degrees, and a common-mode feedback phase margin of 107.8 degrees.

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